# A Bibliography of Publications about the RISC-V Open Source Computer Architecture

Nelson H. F. Beebe
University of Utah
Department of Mathematics, 110 LCB
155 S 1400 E RM 233
Salt Lake City, UT 84112-0090
USA

Tel: +1 801 581 5254
FAX: +1 801 581 4148

E-mail: beebe@math.utah.edu, beebe@acm.org,
beebe@computer.org (Internet)
WWW URL: https://www.math.utah.edu/~beebe/

10 October 2024
Version 2.25

## Title word cross-reference

**#1** [Ano22].

$19\mu W$ [GAE+23]. $^2$ [MRGRCR+21b, PNSD20]. $K$ [LPB+21]. $V_{\min}$ [ZCNA17].

**-Boost** [CPG+23, CRP+23]. **-means** [LPB+21].

**0.37mm2** [WRD+17]. **0.80pJ** [MSZB19]. **0.80pJ/flop** [MSZB19]. **000-core** [DAKK19].

**1** [CSZ+20, DEA+21, DtEt22]. **1-GHz** [CSZ+20]. **1.0** [PCW+22, PCA+24]. **1.24Tflop** [MSZB19]. **1.24Tflop/sW** [MSZB19]. **1.3GHz** [LWA+14]. **1.44** [SWW+22]. **1.44-GHz** [SWW+22]. **1.44GHz** [SWW+21]. **1.46TOPS** [GCL+23]. **1.7** [ZB19]. **1.7-GHz** [ZB19]. **1.89** [WBH+18, WBH+19]. **1.89-GHz** [WBH+18, WBH+19]. **10-bit** [DRC+16]. **12-nm** [LCG+23]. **12-Stage** [CXL+20a]. **12.4TOPS** [CRP+23]. **12.4TOPS/W** [CRP+23]. **123** [IVZV20]. **12nm** [GCL+23]. **136GOPS** [CRP+23]. **140-nW** [TBK+19]. **16** [SCM+21]. **16-bit** [RSA+23]. **16-mm2** [LCG+23]. **16-nm** [BRH+19, RZAH+19b, SWW+22, WBH+18, WBH+19]. **16.7** [LWA+14]. **160mV** [TLB+22]. **16mm2** [GZK+21]. **16nm** [BHR+18, RZAH+19a, SED+23, SWW+21, WRD+17]. **175** [WBH+18, WBH+19]. **175-kHz**

[WBH+18, WBH+19].

**2** [CRP+23]. **2-Petaflop** [SB23]. **2-to-8b** [CRP+23]. **2.0** [HMJ22]. **2.5-D** [PKC+20]. **2.6GFLOPS** [GPV+22]. **2017** [BBdD17, SSB22, TZS+21]. **2019** [GD19, TBL19]. **2021** [IEE21]. **2022** [IEE22]. **2023** [IEE23]. **22-nm** [CSZ+20, ZB19]. **22.1** [CRP+23]. **22nm** [DCC+23, GAE+23, GZK+21, MSZB19, SPDLP+22]. **24th** [BBdD17]. **256** [WYK21]. **256-Bit** [QLC20]. **26th** [TBL19]. **28** [UD20]. **28-nm** [CCA+18a, SAW+20, WSK+20, WCL23, ZCNA17]. **28nm** [LZW+15, ZLP+15, ZCNA16, CCA+18b]. **28th** [IEE21]. **29th** [IEE22]. **2n3m5k** [WRD+17].

**3** [CPLS23, LMP23, TLB+22, VMO+23]. **3-D** [VMO+23]. **3-nW** [TLB+22]. **30** [SB23]. **30-Teraflops** [SB23]. **30-Teraflops/W** [SB23]. **30th** [IEE23]. **32** [KFGH+23]. **32-Bit** [KS22, LCG+23, MLPH23, NHML+22, PMKZ22, DRC+16, DGA+17, GMV20, GSDB18, KM21, LCCS21, MCL22, MMGC20, NKH+21, RSR20, SFGB20, YTÖ21]. **32/64** [MG22]. **32/64-bit** [MG22]. **32I** [MRSBGR+20]. **32IC** [KK21]. **3D** [TEYK21, TYEK21, ZBA+20]. **3D-Graphics** [TEYK21, TYEK21].

**4096-Core** [ZSB21, ZSB20]. **410.0** [KFGH+23]. **410.0-B-32** [KFGH+23]. **45nm** [LWA+14]. **496-Core** [RZAH+19a]. **4MHz** [GAE+23].

**5** [FFW20, FWZL19]. **511-Core** [DXT+18]. **55** [GCL+23]. **5G** [AHB20, BZVCB23, KKH+20, Raj21]. **5G-PUSCH** [BZVCB23].

**6** [TBK+19]. **64** [LWC18]. **64-Bit** [LCG+23, MDPM24, MZZG22, PCO+23, ZB19, CXL+20a, GCL+23, HMTL21, KCGL23, MG22, SGP+23, WSG+21]. **65-nm** [PCO+23]. **65nm** [CCC+22]. **67mm2** [GCL+23]. **695** [RZAH+19a].

**7** [SFGB20]. **7nm** [HMTL21].

**8** [FRC+18]. **8-core** [CKTK22]. **8-to-64** [MSZB19]. **8.2-kHz** [TBK+19]. **8.7mW** [GPV+22]. **89** [DNN23]. **8b** [CRP+23].

**910** [CXL+20a, CXL+20b].

**ABI** [AVS+22]. **Abstraction** [HZS+19]. **Academic** [ABC+20, DCC+23]. **Accelerate** [PMBA19]. **Accelerated** [EAMK21, EKAK22, KFS22, YWZL22]. **Accelerating** [AS18, DEA+21, DtEt22, DAKK19, ERGK21, GTC+20, TSS+22, ZPL+23, KKC+16]. **Acceleration** [ABW+21, AYA+23, CPG+23, CRP+23, DLMP21, FSS20, KSFS24, PLSK20, SB23, Su21, VMFL23, WZW+21, Yan20, KMS22, SCM+21, WWW23]. **Accelerator** [AEAS21, ABW+20, AWB+23, BCCM21, BDdD19b, CCC+19, DNN23, DXT+18, DYZ+22, FHY19, GZK+21, Gra16, GTCS21, JZWL23, JRD+23, KG22b, KYDÖ21, KBBA17, KZH22, LCF23, LNA21, NKH+21, OBSB23, PS22a, PLH+22, PACB21, PGW+20, QLH21, RSRT19, SNH22, TT22, TBR+22, WLI23, WXY+22, YYM21, ZZG21, ZHL+23, DKC+21, RPA22, TZ22, WRD+17, ZPRD21, ZZW+19]. **Accelerators** [ABM+23, GCL+23, HDT+20, KHG20, NHML+22, RHD+23, LWA+14, SFAAL22]. **Access** [MDR19, YWZL22]. **accessible** [APHD22]. **Accuracy** [CLR+21b, CLR+21a, RRC+20, LGB17]. **Accurate** [BHT+21, HGTD20, HGD20b, uhMSI19]. **Achieving** [SZHB21]. **acoustic**

[SGCGCR17]. **Active** [PKC+20]. **Adaptive** [CPG+23, CRP+23, HGTD20, HGTD21, KG22a, TBR+22, TLB+22, LZW+15]. **ADC** [DRC+16]. **Address** [GAMG+23, HYML23, WLW+21]. **Adjacent** [LLL+21]. **AES** [TA22, WYK21, ZPRD21]. **AES-256** [WYK21]. **affordable** [MRGRCR+21a]. **AFTAB** [RRJ+21]. **Against** [GTD+23, KNK+21, DGH19, WSUM19]. **age** [HP18]. **Agile** [HSL+23, HCZ21, LWC+16, PGW+20, XYT+22, XYT+23]. **AGILER** [KG22a]. **AI** [CV22, CPG+23, CRP+23, FRC+18, GMS+23, LCF23, TSABTM20, Yan20, ZJX20]. **AI-extended** [GMS+23]. **AI-IoT** [CPG+23, CRP+23]. **Aimed** [MRAM+23]. **Algebra** [FTRH20]. **Algorithm** [KZH22, LWD20, LPL22, QLH21, RFS20, MRGRCR+21b]. **Algorithms** [ABM+23, dAGM23, MGZ+23, MÇB22, NDZ+21, KMS22]. **All-Digital** [RZAH+19a]. **Alliance** [Ano23b]. **ALU** [RTRM19, RSA+23]. **Always** [EMMB19]. **Always-On** [EMMB19]. **AMS** [APHD21b]. **Analog** [WBH+18]. **Analog/Digital** [WBH+18]. **Analysis** [AKMS20, AKMS21, BHR+18, BRH+19, BB21, CTSG22, DHL+21, DRN+23, HSR+23, HCW23, IK21a, IZG22, KNK+21, LNZ+22, LVPSB+23, NGS20, POMD22, PNV22, SEM19, SSS+22, SML+22, SAW+20, SNOT20, TZS+21, VMO+22, WBH+18, WBH+19, WY23, ZB19, BMM+20, KSAL21, LGB17, RPSD16, SAB24]. **Analyzing** [WSMRM20, YLC21]. **Android** [WWN23]. **ANDROMEDA** [MSR+21]. **ANN** [ZGMD22]. **ANN-based** [ZGMD22]. **AnnikaCore** [ZGL+21]. **Anomaly** [BPS+23, PCL+23, CPL+24]. **API** [SNOT20]. **Application** [DKT+23, GGÁARG+21, HMJ22, LCYK20, LHC+21, LCG+23, PLH+22, WT19, ZB19, ZKS+23, DL17, DAK+21, HH23, TSABTM20]. **Application-Class** [ZB19, DAK+21]. **Application-Specific** [GGÁARG+21, HMJ22, WT19, DL17]. **Applications** [ASE+21, And20, BP21, CRRS22, DNKDN+24, DWG+20, FSMU21, FDMM22, GRCRCG+20, GAO21, HM21, KM21, MLD+23, MPU+23, gMCP19, NBT22, OPY+18, PDLC18, RKH+23, RAPK23, RHD+23, SJR+23, SUM23, SSD+21, SR22, SKK+22, VSD22, WCGL23, ZGG23, ZXXH22, SCR+17, WTY+23, RLL+21]. **applied** [MRGRCR+21a]. **Approach** [LWC+16, MRB+23, MRB+24, NBT22, Suv21a, ZCH+23, PRP+23]. **Approaches** [HSEKD21]. **Approximate** [LGB17, SMOM19, VSD22]. **Approximations** [FFW20]. **Ara** [PCW+22, CSZ+20]. **Ara2** [PCA+24]. **Arbitrary** [AWB+23, JZWL23, ZZQ21]. **Architectural** [KKK+17a, KKK+17b, KKK+17c, MTAL22, MS17]. **Architecture** [ASH19, BP21, CPLS23, COMP19, CLW23, DBP21, DPP22, FHL+22, HBSE22, HYWP+19, HLP+24, HH21, HCP+21, HH22, HMJ24, JSB20, KHG20, KG22a, KG22b, KA20, KNK+21, KKH+20, LCCS21, LF22, LWC18, LHC19, LCW+24, Liu21, LNB+23, MKM20, MR22, MTT21, MAS18, MSJ19, MSD+22, MKVD23, MDR19, NRA+22, NGS20, PDLC18, PS22a, PKN+20, PKC+20, PW17a, PMKZ22, QYZ21, RKH+23, RSA+23, RMP+19, SVM+23, Sew21, SR22, SLB+22, TA22, WLY+22, WAH21, XHY+20, ZSB20, ZSB21, ZHC+18, ZWL+20, ZGL+21, ZZZ21, ZZZ+23, ZNF21, CPL+24, DPV+17, HP18, KSAL21, KHH22, Lu21a, Pat18, PRP+23, RPSD16, Sah23, SCM+21, TCL+21, WTY+23]. **Architectures** [AKMS20, DXT+18, ERGK21, FTRH20, IVZV20, KKK+17a, KKK+17b, KKK+17c, NNPG23, PACB21, SMB17, BF23, CLC+20, GMFC23, LF22, VMFL23]. **Area** [MPU+23, MDR19, PSS23, SSD+21]. **Area-Efficient** [MPU+23]. **ARITH**

[BBdD17, IEE21, IEE22, IEE23, TBL19]. **ARITH-26** [TBL19]. **Arithmetic** [BBdD17, CLR+21b, CLR+21a, GD19, IEE21, IEE22, IEE23, MDPM24, SJM+20, TBL19, SJP+23]. **ARM** [AMRCP21, CRRS21, EHK20, ELG20, FTRH20, IVZV20, KS22, KKE+22, LF22, NGS20, RFS20, SAB24, HLP+24, RMP+19, SNOT21]. **Arm-A** [HLP+24]. **ARM-RISC-V-Heterogeneous** [EHK20]. **ARM64** [TOYK22]. **Armed** [DKT+23]. **Armv8** [Sew21]. **Armv8-A** [Sew21]. **Arnold** [SRD+21]. **Arrow** [AEAS21]. **ARV** [SC17]. **ASIC** [HSEKD21, HM21, KM21, NHML+22]. **ASIC-FPGA** [HM21]. **ASIP** [Ant22]. **Aspects** [AAA+21]. **Assembler** [GSDB18]. **Assembly** [Bor23, Dos19, Smi24, TOYK22]. **Assessment** [GDR+22]. **Assisted** [DBGJ20, ZHX+22, GAMG+23, SMGS22]. **Associativity** [SSS+22]. **AsteRISC** [SLBJ23]. **Asynchronous** [LHT+21, NSM+23, SC17]. **At-Memory** [SB23]. **ATGP_RISC** [MKM20]. **ATGP_RISC-V** [MKM20]. **Atlas** [PW17a]. **Atomic** [WWL+20]. **atrial** [HUL+22]. **Attached** [CMV21]. **Attack** [DHL+21, DBP21, KR24, KNK+21, LHD+21, LHD+22]. **Attacks** [AVS+22, DGH19, GAMG+23, GWZS23, GTD+23, KGBH22, TDH+23, WSUM19]. **Attestation** [SMJ21]. **Augmented** [SRD+21]. **Aurora** [GMFC23, VMFL23]. **Authenticated** [DNKDN+24]. **Authentication** [FdRES23, GLS21]. **Auto** [YCL+23]. **Auto-tuning** [YCL+23]. **Automated** [NSM+23, WXY+22]. **Automatic** [ABM+23, FDS+23, QYZ21, YWZL22]. **Automation** [MKM20]. **Automotive** [CSO+23]. **Autonomous** [DKT+23, RCS+19]. **Autovectorization** [AS22]. **AVR** [KKE+22]. **Aware** [KR24, LHK23, MKB+23, SMB17, SMOM19, LSB22]. **AXI** [EHN23]. **AXI-interconnect** [EHN23]. **AXI4** [DRC+16]. **AXI4-lite** [DRC+16]. **Axiomatic** [HLP+24]. **AxSL** [HLP+24].

**B** [KFGH+23, CPG+23, MZZG22]. **B-Extension** [MZZG22]. **backend** [TMK+16]. **Backup** [PPYB23]. **bad** [FvHC+23]. **Bandits** [DKT+23]. **Bandwidth** [WBH+18, WBH+19, ZZB+20]. **Banshee** [RSS+21]. **Bao** [MP20a, MP20b]. **Baremetal** [MTAL22]. **Barrel** [ABW+20, ABW+21]. **BARVINN** [AWB+23]. **Base** [PMKZ22]. **Baseband** [IFO+18, MB16]. **Based** [ABC+20, AKMS20, Ant22, AMG+20, BFC+23, BP21, BWP22, CXLL22, CDF+20, CYJ+22, CPLS23, DYZ+22, DMR+20, EMMB19, EEI+18, EGBS22, FSPB21, FDS+23, GZC22, GRC+19, GTC+21b, GXLW22, GAO21, GSDB18, HBSE22, HWJ23, HJ23, HCW23, HGLD18, HCZ21, HWG22, JHLD21, JHQ23, KAR+19, KHG20, KG22a, KEAS+18, KRR22, KZH22, LRF+21, LCYK20, LWC18, LHC19, LWD20, LCF23, LXC23, LPL22, LZH20, LLL+21, Lu22, LNB+23, MCL+21, MCL22, MLPH23, MTCL21, MLD+23, MST+23, MSR+21, MKB+23, gMCP19, MDR19, NWP+23, OBB+24, PKC+20, PACB21, PCO+23, POMD22, PNV22, QLH21, QYZ21, QLC20, RSR21, RSR20, RTRM19, RKRF21, RSS+21, RSRT19, RMR21, RHD+23, SJER23, SJM+20, SWWL23, SUAR23, SSB+19, SLB+22, Suv21a, Suv21b, TTB22, TBS+21, TBR+22, UD20, WT19, WZW+21, WWGW23, WCGL23, WMR+22, WWB23, WXY+22, WHB+22, WLC22, WGZ+23, XHY+20, YXH20]. **Based** [YYP+22, ZHC+18, ZWL+20, ZZZ21, ZCH+23, ZUSK23, ZZQ21, ZWL+23, ZSM20, ZSM21, ZS23, ZCNA17, ZNF21, ZZL+22, ZC23, dOTB+20, APSH+22, AvAG21, AFP+17, AS24, ASH19, BCCM21, BHT+21,

CWD+21, Cil21, DBP21, DZZZ23, DRC+16, DGA+17, EAI19, FSMG+19, GRCRCG+20, GTC+21a, GGH+22, GBP21, GGÁARG+21, GLS21, HYXW22, HSL+23, HGD+19, HGPD20, HTGD21, HUL+22, IZG22, KG22b, KM21, KSSMRB23, MRSBGR+20, MRGRCR+21a, MRGRCR+21b, MSFK21, NRA+22, NKH+21, NBT22, RCMQO24, RKH+23, RLL+21, RMP+19, RPA22, RFS20, SGCGCR17, SFAAL22, SSD+21, SJP+23, SJYZ22, SCL+21, SKK+22, TZ22, TDPD+21, WRD+17, WWW23, WW19, WW21, YBR+23, YNYD23, YWZL22, ZPRD22, ZZW+19, ZZB+20, ZGMD22, ZHL+23, CKTG21, IFO+18, KFGH+23, AHB20]. **Basic** [BF23]. **Basis** [HLP+24]. **be** [AP14]. **Behaviour** [BPS+23]. **Benchmark** [MRAM+23]. **Benchmarking** [CGG21]. **Berkeley** [Ano23a]. **Best** [DMR+20, KRR22]. **Between** [HGTD20, EHN23, IK21a]. **Biasing** [CPG+23, CRP+23]. **Big** [MDPM24]. **Big-PERCIVAL** [MDPM24]. **Binaries** [HGLD19]. **Binary** [KCGL23, KGHRM23, RSS+21]. **Bit** [BSSW21, JSB20, KS22, KAMS19, LCG+23, MLPH23, MDPM24, MZZG22, NHML+22, PCO+23, PMKZ22, QLC20, RSR21, ZB19, AS24, CXL+20a, DRC+16, DGA+17, GCL+23, GMV20, GSDB18, HMTL21, KM21, KCGL23, LCCS21, MCL22, MSZB19, MMGC20, MG22, NKH+21, RSR20, RSA+23, SGP+23, SFGB20, WSG+21, YTÖ21]. **bit-interaction** [AS24]. **Bit-Precision** [RSR21]. **Bits** [MTT21]. **BlackParrot** [PGW+20]. **Blake3** [ZPL+23]. **Block** [DPP22, KS22, LCN+23, MCL22, SEM19]. **Blocking** [DDM+20, JHQ23]. **Blocks** [ZWB19]. **Board** [CDF+20, RKH+23, ZSM21, TZPL21]. **Body** [CPG+23, CRP+23]. **BOOM** [Ano23a, BSZ+21, BSZ+24, ZBZ+23]. **BOOM-Explorer** [BSZ+21, BSZ+24]. **Boomerang** [LHK23]. **Boost** [CPG+23, CRP+23]. **Boot** [DBP21, GJC23, HYWP+19, NRLH22, Zha22]. **Bootable** [SGP+23]. **Border** [CDW+24]. **Both** [DMR+20]. **Bottleneck** [KFK+19]. **Branch** [CSM22, SLCK21]. **Bratter** [PKKK22]. **Brew** [Szk21]. **Buffer** [DBGJ20]. **Bug** [RMR21]. **Build** [Szk21]. **Building** [ILG19, LWC+16, WLY+22, ZWB19]. **bulk** [GAE+23]. **bus** [DRC+16]. **bus-based** [DRC+16]. **Byte** [ADF+23, DFA+23].

**C** [MRGRCR+21b, DUM+19]. **Cache** [CKTK22, CKTK23, CCA+18a, DDM+20, GCL+23, HWJ23, HJ23, LHD+21, LCG+23, MKB+23, SSS+22, ZCNA17, GYW+23, ZCNA16]. **Cache-Aware** [MKB+23]. **Cache-Coherent** [GCL+23, LCG+23]. **CADENCE** [RSA+23]. **CakeML** [TMK+16]. **Calib** [ZBZ+23]. **Calibration** [KKH+20]. **Can** [Szk21, PS22b]. **CAN-FD** [PS22b]. **CAP** [CKTG21]. **Capability** [GM21, MMD+22b, MMD+22c]. **Capable** [OBSB23, CIPR21, VTS+23]. **Capacitor** [ZLP+16, LZW+15, MSFK21, ZLP+15]. **Capturing** [TDPD+21]. **carbon** [AFP+17]. **CARE** [DBP21]. **Cars** [Ben23]. **Case** [APSH+22, BHD23, DCM23, GYW+23, HGLD19, HGJD20, PGTD23, RHGD21, SSR+18, WMGD23, YLC21, AP14]. **Case-Study** [APSH+22, BHD23, HGJD20]. **Casting** [KK23]. **Catalog** [HLHK19]. **CCSDS** [IVZV20, KFGH+23]. **Celerity** [DXT+18, RZAH+19b]. **Center** [Ano23g]. **Center-Class** [Ano23g]. **Certificates** [GLS21]. **CFG** [LWLA23]. **CFI** [LWLA23, RSM+23, ZPRD22]. **CGRA** [FGD+19, LNA21]. **ChaCha** [MPP21]. **Challenges** [LVPSB+23]. **Challenging** [NSM+23]. **Changeable** [KIS20]. **Channel** [DGH19, LHD+21, MTAL22, AS24, Bis21, GYW+23]. **Channels** [JHQ23, WSG+21]. **Characteristics** [Lu21b, WY23, ZZZ+23]. **Characterization** [CPWG23, SLK+21, SMMD23]. **Check**

[TA22]. **CHERI** [BPS+23, Sew21]. **CHERI-RISC** [BPS+23]. **Cheshire** [OBSB23]. **China** [Ano23b]. **Chip** [DCM23, DEA+21, DtEt22, FSMU21, GPV+22, GTP+22, Gen24, OBB+24, RLL+21, RZAH+19a, TDPD+21, WSK+20, YLT22, DGA+17, Ano23e, CKTG21, CYJ+22, CRP+23, DNN23, HYWP+19, HZS+19, KSSMRB23, KCHYM19, LNB+23, MSDM23, NKH+21, RSR20, SLK+21, SML+22, SMMD23, SBJ21, ZNF21]. **Chiplet** [KIS20, ZSB20, ZSB21, ZGG23]. **Chips** [DXT+18, SG23, ZJX20]. **Chisel** [IK21a, XLZ23, ZCH+23]. **Chisel-Based** [ZCH+23]. **Choice** [HSR+23]. **CIFER** [LCG+23, ZPRD23]. **Cimone** [BFP+22]. **Cipher** [KS22, MCL22, TGMD21]. **Circuit** [WZW+19, KKC+16]. **Circuitry** [BBV+23]. **circular** [HC20]. **circular-shift** [HC20]. **CLARINET** [SJM+20, SJP+23]. **Class** [Ano23g, ZB19, DAK+21]. **Classes** [FAPHD23, JHQ23]. **Classic** [PGZMG21]. **Classical** [KGHRM23]. **Classification** [PLSK20]. **classifier** [SGCGCR17]. **CLIC** [MTCL21]. **Clocked** [PNV22]. **clocking** [LZW+15]. **Closed** [RHD+23]. **Closed-loop** [RHD+23]. **Closing** [HGD20a]. **Cloud** [CXL+20b, Su20, AAC+23, LF22]. **Cluster** [GPV+22, GTP+22, KMB22, MRB+23, MRB+24, NRB+23]. **Clustering** [LPB+21]. **Clustering-specific** [LPB+21]. **Clusters** [GRC+19]. **CMOS** [CKTK22, CKTK23, CCA+18a, CCA+18b, GAE+23, NWP+23, PCO+23, RZAH+19a, SED+23, WCL23]. **CNN** [GDR+22, HCL+21, LHC+21, LHC19, PLH+22, PMBA19, QLH21, SFAAL22, WLI23, WWX+24, WLC22, YYP+22, ZZG21]. **Co** [AvAG21, BPS+23, CPLS23, FSMG+19, HSL+23, HMJ22, Liu21, uhMSI19, POMD22, RFS20, WBH+18, ZWL+23, ZNF21, GAE+23, HP18, KHH22, RPD+15, YWZL22]. **Co-Design** [HMJ22, uhMSI19, RFS20, ZWL+23, ZNF21, BPS+23, HSL+23, Liu21, HP18]. **Co-Design-Based** [POMD22]. **Co-Designed** [WBH+18]. **Co-Processor** [CPLS23, AvAG21, GAE+23, KHH22, RPD+15, YWZL22]. **Co-Processors** [FSMG+19]. **Code** [GTD+23, HYML23, TA22, ZPRD23, TOYK22]. **Codes** [KGHRM23, TS20, WTS21]. **Coherent** [GCL+23, LCG+23]. **ColibriES** [RHD+23]. **Collaborative** [DYZ+22, YLT+23]. **Commercial** [CXL+20a, HSEKD21]. **commit** [HK20]. **Communication** [KIS20, PS22b, ZSM20, HC20, TCL+21]. **Communications** [RMF22]. **Compact** [DNN23, TBR+22, MRSBGR+20]. **Comparative** [CPWG23, IK21a, KSAL21, DAK+21]. **Comparison** [BWP22, ET21, HSEKD21, PNG20, WYK21, CRRS21, SCR+17]. **COMPAS** [SMGS22]. **CompaSeC** [GAMG+23]. **Compatible** [BBVB20, HLHK19, RKRF21, SGP+23, BGVB18, ETR+20, WRD+17]. **Compilation** [TZS+21]. **Compiler** [AS22, DCL23, GAMG+23, KR24, PNG20, SMGS22, WXY+22, TMK+16]. **Compiler-assisted** [GAMG+23, SMGS22]. **Complete** [FHL+22, WMR+22]. **Completion** [UD20]. **complexity** [NKTS23]. **Compliance** [BHGD21, HGD20a, HTGD21]. **Compliant** [KGC+24, PCA+24]. **Components** [ABC+20]. **Composable** [ZWB19]. **Comprehensive** [SAB24]. **compressed** [KK21]. **Compressor** [IVZV20]. **Compromising** [Bis21]. **Computation** [GFB+24, uhMSI19, WWX+24]. **Computational** [MST+23]. **Computations** [Ant22]. **Compute** [CKTK22, CKTK23, DAKK19, GTP+22, LCG+23, SZHB21]. **Computer** [Ano22, BBdD17, HLP+24, HH21, HCP+21, HH22, IEE21, IEE22, IEE23, KG22c, LF22, MSJ19, MKVD23, PH17, PH21, RKH+23, TBL19, TSW+23, HP18, Pat18, TZPL21].

**Computers** [BFP+22, KIS20, Pat17]. **Computing** [BDdD19b, CSM+21, CXL+20b, DYZ+22, FGD+19, FSMU21, GRC+19, ILG19, KBBA17, LWC18, MDPM24, MPU+23, NPA+23, PCW+22, PPYB23, SJBS21, TBSH22, WLW+21, XZW+22, Yan20, ZSB20, ZSB21, ZHL+23, Gre20, HYXW22, SCM+21, WWL+20, WTY+23, YWZL22]. **Computing-in-Memory** [ZHL+23]. **Concolic** [HGLD19]. **Conference** [GD19, IEE21, IEE22]. **Confidential** [XZW+22]. **Configurable** [BHT+21, HGLD18, KGC+24, KEAS+18, PKN+20, RRJ+21, TGRK21, ZS23, APHD22, HYXW22, HGPD20]. **Configuring** [FSMU21]. **Considered** [PW17b]. **Constrained** [APHD21a, ET21, dAGM23, JBK23, SMJ21, ZHLR22, SCL+21]. **Constraint** [FDS+23]. **Constraint-Based** [FDS+23]. **Constraints** [LHT+21, ZPRD21]. **Construction** [MCL+21]. **Consumption** [MTT21, MRAM+23, TDH+23, ZCH22]. **context** [LSB22]. **context-aware** [LSB22]. **Continual** [RRC+20]. **Control** [Ant22, ABW+20, KKH+20, PSM23, RLL+21, RHD+23, YLT+23, ZGG23, PKKK22, Sah23, ZPRD23]. **control-flow** [PKKK22]. **Controlled** [AWB+23, FFW20, SNH22]. **Controller** [DNKDN+24, EAI19, GRCRCG+20, MST+23, MDR19, OBB+24, Suv21a, SKK+22, TL22]. **Controllers** [ZZG21]. **ControlPULP** [OBB+24]. **Conversion** [DCM23, RPD+15]. **Converters** [ZLP+16, LZW+15, ZLP+15]. **Convolution** [KSAL21, WZW+21, RCMQO24, TZ22]. **Coprocessor** [BDdD19a, CMV21, DEC+18, FSMU21, HCL+21, LHC+21, LKKK22, LYL23, MPU+23, PSS23, SWWL23, WWGW23, ZWL+20, GBP21, PRS+15]. **Coprocessors** [CSM+21, LVR+20]. **CORDIC** [NKH+21, YYM21]. **CORDIC-based** [NKH+21]. **Core** [ASE+21, BBV+23, BZVCB23, BP21, CXL+20a, CKTK23, COMP19, DXT+18, EHK20, GST+17, GZK+21, GTD+23, GCCR21, GCR+23, HWJ23, HSR+23, HCP+21, HM21, IK21a, KHG20, KG22a, KM21, KKOY19, KSRT23, LRF+21, LKKK22, MMD+22a, MMD+22b, MMD+22c, MRAM+23, NWP+23, NKTS23, OBB+24, PDLC18, PLH+22, PAPJ+23, PCA+24, PMKZ22, PS22b, PMBA19, RZAH+19a, SGP+23, SAF+23, SLBJ23, SWW+21, SWW+22, SR22, SUAR23, SFGB20, SKK+22, TGRK19, TGRK21, VSD22, WLI23, WSG+21, WSK+20, WLC22, YLC21, YTÖ21, ZB19, ZSB21, dOTB+20, BCM+21, CKTK22, CYJ+22, DAKK19, EHN23, FvHC+23, GG18, HMTL21, Lu21b, MRSBGR+20, SJYZ22, TH22, WRD+17, WTY+23, ZSB20, ZPRD21, ZPRD23, HHTo23]. **core-based** [SJYZ22]. **CORE-V** [HHTo23]. **Cores** [ARH+22, BPM+21, BPF+22, CSM+21, Cho18, Cho19, ET21, FSPB21, FGD+19, GMS+23, GGÁARG+21, GRD22, HHB+19, JHL+21, JS23, KIS22, KG22c, LCG+23, MLPH23, NPA+23, OCMP19, OCC+17, SSR+18, SZHB21, SB23, Bar20, SBJ21, SCR+17]. **Core** [Ano23f]. **Correction** [Cho19, KFGH+23, KGHRM23, UD20, ZC23]. **Correlation** [DHL+21]. **Corruption** [BR24, CDW+24]. **Cost** [BPM+21, DCL23, RKH+23, RMR21, SG23, SLZ+20, ZB19, ZG22, HWG22, RAPK23]. **Cost-effective** [ZG22]. **COTS** [dOK23]. **Countermeasure** [DHL+21, GAMG+23]. **Countermeasures** [GTD+23, LBDPP19]. **Counters** [DRN+23]. **Coupled** [GKB+22, CMV21, JZWL23]. **Course** [LLS22]. **Coverage** [AKMS21]. **Covert** [MTAL22]. **Coyote** [PFD21]. **CPA** [TDH+23]. **CPK** [ZS23]. **CPU** [AWB+23, CWD+21, COMP19, GG18, IZG22, LKKK22, MCL22, MKČ23, MTAL22,

MS17, Pat18, RKRF21, SNH22, SSB22, Szk21, WLC22, ZZZ21]. **CPU(R)** [TZS+21]. **CPUs** [CPWG23, GWZS23, HWJ23, JRW+23]. **Critic** [RBK18]. **Critical** [MKČ23, RLL+21, SKK+22, WMA+21]. **criticality** [CIPR21]. **Cross** [HGJD20, VOK+22, WWN23, APHD22]. **Cross-layer** [VOK+22]. **Cross-Level** [HGJD20, APHD22]. **Cross-Platform** [WWN23]. **Crypto** [KR24, RFS20]. **Cryptographic** [Bis21, DHL+21, HDT+20, MLPH23, MÇB22, SNK22, TDH+23, ZWL+23]. **Cryptography** [dAGM23, KGHRM23, LKKK22, NDZ+21, NHML+22, TGMD20, XHY+20, ZKS+23]. **Cryptoprocessor** [HBSE22, ZHC+18]. **Cryptosystem** [PGZMG21]. **CRYSTALS** [GJC23, NDZ+21]. **CRYSTALS-Dilithium** [GJC23]. **CSR** [BHGD21]. **Current** [AMG+20, HCW23]. **Custom** [CWS+24, DFA+23, HHB23, LHC19, LMP23, MRB+23, MRB+24, NKH+21, SNH22, Su21, WWX+24, PKL21, PJL21]. **Customizable** [SCM+21]. **Customized** [WZW+21, EHN23]. **Customizing** [MMD+22a]. **CV32A6** [HH23]. **CVA6** [MMD+22a, MTAL22, SVM+23]. **Cyber** [APHD21b, Ano22]. **Cyber-Physical** [APHD21b]. **Cyber-Security** [Ano22]. **Cycle** [GGH+22, uhMSI19, ZNF21, DPV+17, UD18]. **Cycle-Accurate** [uhMSI19]. **Cycle-True** [ZNF21].

**D** [PKC+20, VMO+23]. **D2** [PGTD23]. **DARKSIDE** [GTP+22, GPV+22]. **Data** [Ano23g, DAKK19, FHL+22, GLS21, KRR22, KGBH22, KK23, LWC18, LVPSB+23, RKRF21, Su21, TBS+21, ZHL+23, RPD+15, ZZB+20]. **Data-Flow** [FHL+22]. **dataflow** [GAE+23, YWZL22]. **Datapath** [HMJ24]. **Datapaths** [VROdlT22]. **Day** [CPL+24]. **DBPS** [LCN+23]. **DC** [LZW+15, WCL23, ZLP+15, ZLP+16]. **DC-DC** [LZW+15, ZLP+15]. **DCLS** [NKTS23]. **DCT** [HHB23]. **De-RISC** [WMA+21, WMR+22]. **Deblocking** [AS18]. **Debug** [LKHK23]. **Debugger** [RSR20]. **DECADES** [GCL+23]. **Decentralized** [GLS21, NBT22, SLMS21]. **Decimal** [uhMSI19]. **Decoder** [KFGH+23, SUAR23]. **Decoupled** [Ant22, MPU+23]. **Decryption** [AYA+23]. **dedicated** [BMM+20]. **Deep** [ABW+21, CRRS22, FHY19, HSL+23, KSAL21, SLCK21, TBR+22, CRRS21, RCMQO24]. **Deeply** [JZWL23, QCL+23]. **Deeply-coupled** [JZWL23]. **Deflection** [KG17]. **Deflection-Routed** [KG17]. **delay** [LSB22]. **delegated** [CLM+22]. **Demonstrating** [PKL21]. **Dependable** [MSDM23, NPA+23]. **Deployment** [BCCM21]. **Depth** [KNK+21]. **Design** [BSZ+21, BSZ+24, CWD+21, CPLS23, Chi23, Chi24, CTSG22, DXT+18, DYZ+22, DZZZ23, FHD22, GZ22, GMS+23, GGH+22, GBP21, GXLW22, GKB+22, GMV20, GRD22, HWJ23, HSR+23, HH21, HH22, HYXW22, HSWM23, HMJ22, HGD+19, IK21a, KM21, LHC19, LCF23, LYL23, LHK23, LLS22, LZH20, LLL+21, Lu22, MCL22, MLPH23, MSSS23, MZZG22, uhMSI19, Mis22, NKTS23, NSM+23, NRLH22, OPY+18, OCMP19, PDLC18, PKC+20, PAPJ+23, PGTD23, PH17, PH21, PCW+22, POMD22, PSZMM21, PNV22, QLC20, RSA+23, RFS20, RCS+19, SGP+23, SVM+23, SLBJ23, SJER23, SWWL23, SSB+19, SFGB20, SS22, TMR+19, TGT+23, WLY+22, WWGW23, WTY+23, YBR+23, YNYD23, YLT+23, YTÖ21, ZTC21, ZHC+18, ZWB19, ZGL+21, ZZZ21, ZGG23, ZZQ21, ZWL+23, ZNF21, BMM+20, BCM+21, Bar20, BPS+23, HSL+23, HP18, LF22, Liu21, RPSD16, SJYZ22]. **Designed** [Ano22, MMGC20, QLH21, WBH+18, DDM+20, ZZW+19]. **Designing**

[CSM+21, KGC+24, MSJ19, Chi23]. **Designs** [CPWG23]. **Detection** [GKB+22, HSWM23, HUL+22, HCL+21, LRF+21, LHD+21, LHC+21, LCF23, LXC23, PCL+23, PGTD23, UD20, CPL+24, KSAL21, LHD+22, SJYZ22, ZZW+19]. **Detection-Based** [UD20]. **Developing** [JHL+21, PCL+23, PHC+23, TSABTM20, XYT+22, XYT+23]. **Development** [And20, CRMR+23, CPL+24, EHN23, HCW23, SNM22, Suv21a, SKK+22, ZCH+23, Bar20, PKL21]. **Developments** [AAB+23]. **Device** [Lu21b, SB23, WHB+22]. **Devices** [ASH19, CWS+24, GST+17, HCL+21, JBK23, MRAM+23, MTJ+22, NPA+23, SMJ21, CTN18, EHN23, SCL+21]. **DFT** [ZCH+23]. **Diagnostic** [MGZ+23]. **Differences** [Cho18, Cho19]. **Different** [AKMS21, KIS22]. **Digit** [HSE+24]. **Digital** [CCC+19, GLS21, GJC23, HH21, HH22, HSEKD21, RZAH+19a, KSSMRB23, TCL+21, Ano23f, WBH+18]. **Dilemma** [HCW23]. **Dilithium** [GJC23]. **Direct** [JRW+23, MDR19]. **Directional** [KG17]. **Disassembler** [GSDB18]. **Discussion** [APHD21a]. **dispatch** [HK20, KKC+16]. **DIV** [LGB17]. **Division** [HSE+24]. **DNA** [WHB+22]. **DNN** [AWB+23, ADF+23, CTN18, CPG+23, CRP+23, GPV+22, GTP+22, HM21, KSAL21, LCN+23, OGT+20, WXY+22]. **DOJO** [TSW+23]. **Domain** [HP18, OBSB23, XHY+20, ZXXH22, Pat18]. **Domain-Specific** [OBSB23, XHY+20, ZXXH22, HP18, Pat18]. **Domains** [DMR+20]. **Domestic** [WLC22]. **Dot** [KBBA17]. **double** [LWA+14]. **double-precision** [LWA+14]. **Driven** [DWG+20, MRB+23, MRB+24, FHD22, LKHK23, RCS+19, gMCP19]. **Drones** [Ben23]. **Drop** [HLHK19, YLT22]. **Drop-In** [HLHK19]. **DSP** [GST+17, LWD20, LYL23, Su21]. **Dual** [CYJ+22, HMTL21, KSRT23, SUAR23, WSK+20, EHN23, GMV20, NKTS23]. **Dual-Core** [SUAR23, WSK+20, CYJ+22, HMTL21, EHN23]. **Dual-Issue** [KSRT23]. **dummy** [LSB22]. **DuVisor** [CLM+22]. **DVFS** [TBK+19, TLS22]. **DVINO** [CCC+22]. **Dynamic** [BDdD19a, CMV21, CKTG21, DHL+21, KCGL23, LCN+23, PDLC18, TBK+19, TCH23, WW21, ZWL+20, PRP+23]. **Dynamically** [QLC20].

**E203** [SJYZ22]. **Early** [HGLD19, LNZ+22, ZGD22]. **ECG** [HUL+22]. **Ecosystem** [AAA+21, EAM+22, uhMSI19, PNG20, TZPL21]. **ECU** [ZS23]. **ECUs** [CTSG22, CSO+23]. **EDA** [GG18]. **Edge** [AYA+23, CSM+21, CXL+20b, FRC+18, FSMU21, GPV+22, GTP+22, HSR+23, LCF23, MST+23, MTJ+22, NPA+23, OGT+20, RRC+20, Su20, TTB22, WWX+24, WCGL23, Yan20, GRC+19, SCM+21, WTY+23, Raj21, CV22]. **Edge-AI** [CV22]. **Edge-Computing** [CSM+21]. **Edition** [HH22]. **Education** [HCP+21, MSJ19, MKVD23, APHD22]. **Educational** [SUM23]. **EEG** [LCF23]. **EEG-based** [LCF23]. **Effect** [AKMS20, CLWL21, RCK+24]. **effective** [ZG22]. **Effects** [Cho18, Cho19, TAC+22, dOTB+20]. **Efficiency** [CPWG23, CLR+21b, CLR+21a, dAGM23, MAS18, LGB17, SAB24, WWZL17]. **Efficient** [AHB20, BZVCB23, CSZ+20, DFA+23, DWG+20, EGBS22, GTC+21a, GTC+21b, HMJ24, HGJD20, IK21b, KIS22, KSRT23, LCN+23, MLD+23, MKB+23, MPU+23, PCW+22, PCA+24, RFS20, SNH22, SUAR23, TBSH22, ZZZ+23, ZKS+23, CSM22, EHN23, HUL+22, HCL+21, ZSB20]. **eFPGA** [GCL+23, LCG+23, SRD+21]. **eFPGA-Augmented** [SRD+21]. **EHE** [EGBS22]. **Eight**

[CKTK23, SWW+21, SWW+22]. **Eight-Core** [CKTK23, SWW+21, SWW+22]. **Electronics** [SKK+22]. **Elementary** [CWS+24]. **elevate** [TZPL21]. **Embedded** [AvAG21, BCCM21, DBGJ19, DBGJ20, DK23, FSMU21, dAGM23, HGLD19, HWG22, JK20, KLP+20, KKOY19, KSRT23, LKHK23, MSP23, MTCL21, MZZG22, RAPK23, RHD+23, SMP22, SG23, SUM23, SAB22, SLB+22, TL22, WLI23, ZZG21, ZGMD22, ZGD22, ZHX+22, Ano20, DZZZ23, GAE+23, KKC+16, MP20a, MP20b, SFAAL22, ZJX20, ZG22]. **Emission** [SG23]. **Emoji** [BJN23]. **Emotion** [LCF23]. **Empiricism** [SJM+20, SJP+23]. **EMS** [GG18]. **emulated** [MRGRCR+21b]. **Emulates** [LKHK23]. **Emulation** [CRMR+23, KEAS+18, OBB+24, PPYB23, ZZB+20, ZUSK23]. **Emulator** [LRB18]. **En/Decryption** [AYA+23]. **Enable** [PFD21]. **Enabled** [TGRK19, TGRK21, SJP+23]. **Enabling** [CKTG21, FSMU21, GTC+21a, GTC+21b, MS17]. **Enclave** [SJBS21]. **Encoder** [KKEG22, ZPRD22, WWW23]. **Encryption** [AYA+23, Cil21, FdRES23, Lu22, PS22a, YXH20]. **End** [CPG+23, GM21, GTC+21a, GTC+21b, KHS+23, SRD+21]. **End-Node** [CPG+23]. **End-to-End** [GM21, KHS+23]. **Endpoint** [CWS+24, GST+17]. **Energy** [CSZ+20, CPWG23, DWG+20, ET21, FGD+19, GTC+21a, GTC+21b, HMJ24, HCL+21, KIS22, KSRT23, MTT21, MKB+23, MRAM+23, SNH22, WT19, ZB19, SAB24, WWZL17]. **Energy-Efficient** [CSZ+20, DWG+20, HMJ24, KIS22, KSRT23, MKB+23, SNH22, HCL+21]. **Enforcement** [FHL+22]. **Engine** [ERGK21, YXH20]. **Engineering** [Sew21]. **enhanced** [HP18]. **Enhancement** [KK23]. **Enhancing** [ZKS+23]. **entropy** [SNM22]. **Environment** [BCZ21a, HDT+20, KHS+23, MCL+21, NSM+23, OCMP19, SNK22, SNOT21, BMM+20]. **Environments** [AVS+22, SMMD23, SGCGCR17]. **Epilepsy** [HSWM23, HCL+21, LHC+21]. **Error** [Cho18, Cho19, DXYZ19, GDR+22, GKB+22, KFGH+23, KGHRM23, LNZ+22, SJER23, UD20, VSD22, WCL23, YLC21, ZC23]. **Error-Correction** [KFGH+23, KGHRM23]. **Error-Resilient** [WCL23]. **Error-Tolerant** [VSD22]. **Errors** [ARH+22, FKS22]. **Esperanto** [DEA+21, DtEt22]. **Establishment** [DNKDN+24]. **Estimation** [KMB22, ZGMD22, ZGD22]. **ET-SoC-1** [DEA+21, DtEt22]. **ETC** [ZSM21]. **Ethereum** [GLS21, SLMS21]. **Ethernet** [CRMR+23]. **Ethical** [HSR+23]. **Europe** [AAC+23]. **European** [FDMM22]. **Evaluate** [VOK+22]. **Evaluating** [IVZV20, KCGL23, MAS18, MTJ+22, RZAH+19b, SNK22, dOTB+20, dOK23, GYW+23]. **Evaluation** [AS22, APHD21a, APHD21b, AMRCP21, BSSW21, CG23, DAPS21, DDM+20, FTRH20, FHD22, GMFC23, HJ23, HLHK19, HGD20b, HHB+19, ISM+23, JBK23, JS23, KIS22, uhMSI19, MÇB22, PPYB23, SSB22, TMR+19, ZZZ+23, AS24, FKS22, HGTD21, VMFL23]. **Even** [Szk21]. **Event** [BWZ+21, CLWL21, EGBS22, MST+23, MRB+23, MRB+24, Suv21b]. **Event-Based** [MST+23]. **Event-Driven** [MRB+23, MRB+24]. **Everyone** [RBK18]. **Exa** [TSW+23]. **Exa-Scale** [TSW+23]. **Exact** [KBBA17]. **Executed** [ZPRD23]. **Execution** [AVS+22, BCZ21a, BHD23, CDW+24, GZ22, GCCR21, GCR+23, HDT+20, IZG22, MCL+21, MAS18, SNOT21, TZG+23, ZHX+22]. **Experimental** [FKS22]. **Experiments** [CLC+20, CRRS21]. **exploiting** [TLS22, ZNF21]. **Exploration** [BSZ+21, BSZ+24, GRD22, HJ23, KG22c, LHK23, MSR+21, SVM+23, SLBJ23, TAC+22]. **Explorer** [BSZ+21, BSZ+24]. **Exploring** [CMV21, Lu21b, MDPM24, PCA+24, PGZMG21, RBK18, SG23, PJL21].

**Exposed** [HMJ24]. **Exposing** [TBS+21]. **ExSdotp** [BPF+22]. **Extend** [WZW+19]. **Extended** [GM21, GFB+24, JHLD21, KK23, MR22, SED+23, TCL+21, WLI23, AS24, GMS+23, HYXW22]. **Extending** [AS18, AHB20, FSS20, PS22b, PMBA19, TEYK21, TYEK21, VROdlT22, ZPRD21]. **Extensible** [HGLD18, HGPD20]. **Extension** [ABP22, AHV+21, BKdLSGL23, BPF+22, CLC+20, CXL+20a, DAHK20, DCL23, GZC22, GFB+24, HVW+21, HCZ21, ISM+23, JSB20, JZWL23, KA20, KKOY19, KZH22, KFGH+23, KGHRM23, MCL+21, MC22, MTCL21, MZZG22, NDZ+21, PPS+19, PGZMG21, PSM23, RSR21, RMF22, SZHB21, TGMD20, TGMD21, WWL+20, WLW+21, WY23, YCL+23, ZHC+18, ZXXH22, ZKS+23, MB16, PKKK22, TZ22, VMFL23]. **Extensions** [CLW23, DBGJ19, FHD22, GTC+20, GST+17, dAGM23, GMK+23, KAMS19, LCN+23, LMP23, SPDLP+22, Su21, SNK22, YYP+22, MMR+17, TMR+19, ZJX20]. **Extraction** [GTD+23, LWLA23]. **Extreme** [GPV+22, GTP+22, OGT+20, RRC+20, TTB22, SCM+21]. **Extreme-Edge** [GPV+22, GTP+22, OGT+20, RRC+20, SCM+21].

**Fabric** [DXT+18]. **Factors** [TDH+23]. **Fail** [TDPD+21]. **Fail-Reason** [TDPD+21]. **Families** [FDS+23]. **Fast** [BHT+21, DXT+18, HGTD20, HGD20b, MTCL21, MGZ+23, MMA+18, PLSK20, RSS+21, KHH22, WWZL17]. **faster** [CRRS21]. **Fault** [AKMS20, AMRCP21, BWZ+21, BMM+20, BCM+21, DKA+22, ELG20, GAMG+23, KR24, KNK+21, LBDPP19, gMCP19, POMD22, RMP+19, SLZ+20, SML+22, SMMD23, SMGS22, SR22, SUAR23, TAC+22, WW19, WW21, dOK23, JS23]. **Fault-Safe** [gMCP19]. **Fault-Tolerance** [RMP+19]. **Fault-Tolerant** [SLZ+20, SML+22, SMMD23, SR22, SUAR23, dOK23]. **Faults** [YLC21]. **Faulty** [AVS+22]. **FD** [CSZ+20, KCZ+17, MSZB19, PS22b, SAW+20, SPDLP+22, WSK+20]. **FD-SOI** [CSZ+20, KCZ+17, MSZB19, SAW+20, SPDLP+22, WSK+20]. **FDSOI** [DCC+23, UD18, UD20, ZB19, ZLP+15, ZLP+16]. **features** [MS17]. **Featuring** [GCR+23, DGA+17]. **FemtoRV32** [NWP+23]. **FFT** [JZWL23, VMFL23, WRD+17, ZZQ21]. **Fi** [WRD+17]. **fibrillation** [HUL+22]. **Field** [KGHRM23]. **Files** [Ano21]. **Filter** [AS18]. **Fine** [NRB+23, RSM+23, SAW+20, WSK+20, NKTS23]. **Fine-Grain** [NRB+23, WSK+20]. **Fine-Grained** [SAW+20, RSM+23, NKTS23]. **FinFET** [BHR+18, BRH+19, GCL+23, GZK+21, HMTL21, SWW+21, SWW+22, WRD+17, WBH+18, WBH+19, GAE+23]. **FIRECAP** [TDPD+21]. **FireSim** [FHY19]. **Firmware** [HGD+19, BCZ21b]. **First** [BFP+22, Gen24, SMP22, WMA+21]. **Five** [PMKZ22, CSM22]. **Five-Stage** [PMKZ22]. **Fixed** [Liu21, YCL+23, ZG22]. **Fixed-point** [Liu21, YCL+23, ZG22]. **FIXER** [DBGJ19]. **Flash** [BFC+23]. **Flash-Based** [BFC+23]. **FlexBex** [DAHK20]. **Flexible** [GTC+21a, GTC+21b, KKH+20, RSR20, SRD+21, Su21, DKC+21]. **Flip** [BWZ+21]. **Flip-Flops** [BWZ+21]. **Floating** [Ano20, BPM+21, CSZ+20, GFB+24, MSZB19, PSS23, PCO+23, SEG20, ZSB20, ZSB21, PRS+15, YWZL22, BDdD19b]. **Floating-Point** [Ano20, BPM+21, CSZ+20, MSZB19, PSS23, PCO+23, SEG20, ZSB21, ZSB20, YWZL22, BDdD19b]. **flop** [MSZB19]. **Flops** [BWZ+21]. **Florian** [PHC+23]. **Flow** [Ant22, DBGJ19, FHL+22, KMB22, PDLC18, PKC+20, SS19, SSB+19, WGZ+23, ZPRD23, MRSBGR+20, PKKK22, Sah23, SJYZ22]. **FMA** [QCL+23]. **Forecasting** [CDF+20]. **Forest** [TTB22]. **Forest-Based** [TTB22].

**Formal** [CAL23, DMR+20, FAPHD23, GM21, Sew21, TBLD23, TAC+22, WMGD23, XLZ23]. **FortiFix** [KR24]. **forward** [PKKK22]. **Four** [GZ22, LCG+23]. **Four-Stage** [GZ22]. **FP16** [TBR+22]. **FPGA** [APSH+22, BCCM21, CMV21, CKTG21, Cil21, DPV+17, DDM+20, DXYZ19, EAI19, FvHC+23, GAO21, GMV20, Gra16, GSDB18, HHB23, HCP+21, HSWM23, HM21, IFO+18, JSB20, KHG20, KG22b, KFGH+23, LCYK20, LCF23, MCL22, MLPH23, MFM+19, MSJ19, MSR+21, NHML+22, OBB+24, PLSK20, PSZMM21, QLC20, SUM23, SSB+19, SSD+22, TLS22, WSMRM20, WHB+22, WLC22, YLT+23, ZUSK23, ZCH22, ZC23, dOTB+20, dOK23]. **FPGA-Based** [CKTG21, IFO+18, KFGH+23, OBB+24, ZUSK23, APSH+22, Cil21, KG22b]. **FPGA-Optimized** [MFM+19]. **FPGAs** [BFC+23, HHB+19, KAR+19, KG17, MAS18, RTRM19, WW19, WW21, WWB23, ZZB+20]. **FPU** [BPM+21, KGC+24, PHC+23]. **Framework** [BSZ+21, DKA+22, EEI+18, GMS+23, KR24, KEAS+18, LKHK23, LNA21, LHK23, MSJ19, MSR+21, NRA+22, SSR+18, SJM+20, SSD+22, ZBZ+23, ZNF21, APHD22, BCZ21a, MS17, MRGRCR+21a, SJP+23, SCL+21]. **frameworks** [KSAL21]. **Fraud** [GLS21]. **Free** [DPP22, AP14]. **FreeBSD** [Hor20]. **FreeBSD/RISC** [Hor20]. **FreeBSD/RISC-V** [Hor20]. **Freedom** [Ano21]. **Frequency** [DHL+21]. **Frequent** [MTT21]. **FrodoKEM** [KFS22]. **fruit** [KSAL21]. **Full** [BHT+21, SZHB21, Sew21]. **Full-Platform** [BHT+21]. **Full-scale** [Sew21]. **Fully** [HC20, PS22a, WCL23, ZHL+23, Ano20]. **Fully-Homomorphic** [PS22a]. **Fully-Parallel** [ZHL+23]. **Function** [GZC22]. **Functional** [ASE+21, JRD+23, LPZ19, YLC21, MRSBGR+20, SC17]. **Functions** [BKdLSGL23, CWS+24, LMP23]. **future** [AAC+23, TCL+21]. **Fuzzerfly** [RCK+24]. **Fuzzing** [RCK+24].

**Galois** [KGHRM23]. **GaN** [RLL+21]. **GaN-Applications** [RLL+21]. **Gap** [BB21, HGD20a, HM21, FRC+18]. **GAP-8** [FRC+18]. **Gateway** [CXLL22]. **Gateways** [RRJ+21]. **gem5** [RSRT19]. **GEMM** [RCMQO24]. **GEMM-based** [RCMQO24]. **General** [SNOT21, MRGRCR+21b, TZ22]. **general-purpose** [TZ22]. **Generated** [BHR+18, SBJ21]. **Generating** [EEI+18, GGÁARG+21, SBJ21]. **Generation** [BFP+22, FSPB21, FDS+23, GLS21, GD19, LNA21, LPZ19, TH22, TBLD23, Ben23, CSO+23]. **Generator** [Ano23e, Ant22, BRH+19, CKK+18, MKM20, TS20, TTDD21, WTS21, LSB22, SBJ21]. **Generic** [GTCS21, OPY+18, RKH+23]. **Genome** [LVPSB+23]. **Genotype** [MRB+23, MRB+24]. **Gesture** [ZWL+20]. **Getting** [Hor20]. **GFLOPS** [LWA+14]. **GFLOPS/W** [LWA+14]. **GHz** [CSZ+20, RZAH+19a, SWW+22, SPDLP+22, WBH+18, WBH+19, ZB19]. **Giga** [GCL+23, RZAH+19a, RZAH+19b]. **Giga-RISC-V** [RZAH+19b]. **Global** [WLW+21]. **GlobalPlatform** [SNOT20]. **Go** [SC17]. **GoblinCore** [LWC18]. **GoblinCore-64** [LWC18]. **golden** [HP18]. **GOPS** [GZK+21]. **GOPS/W** [GZK+21]. **GOST** [DNN23]. **GOST-28147-89** [DNN23]. **GPC** [LNB+23]. **GPGCN** [TZ22]. **GPGPU** [ETR+20, TEYK21, TYEK21]. **GPUs** [TSS+22]. **Grade** [WMA+21, WMR+22]. **Grain** [NRB+23, VROdlT22, WSK+20]. **Grained** [SAW+20, NKTS23, RSM+23]. **granularity** [HYXW22]. **Graph** [DYZ+22, Sah23, TZ22]. **Graphic** [TSS+22]. **Graphics** [TEYK21, WY23, TYEK21, ZJX20]. **Grid** [CYJ+22, SLMS21, TS20, WTS21]. **GRVI**

[Gra16]. **GVSoC** [BHT+21].

**H.265** [AS18]. **H.265/HEVC** [AS18]. **HAMSA** [KSRT23]. **HAMSA-DI** [KSRT23]. **Hardened** [DAPS21]. **Hardened-by-Replication** [DAPS21]. **Hardening** [MSDM23]. **Hardware** [AKMS20, ABM+23, ARH+22, Ant22, AHV+21, Bau17, BPF+22, BPS+23, CTSG22, DBGJ20, DCM23, DYZ+22, DLMP21, EMMB19, EGBS22, FSS20, Gen24, GWZS23, GMK+23, HVW+21, HSL+23, HLHK19, KFS22, KSFS24, KEAS+18, KYDÖ21, KBBA17, Lu21a, MCL+21, uhMSI19, NRA+22, NKH+21, OBB+24, PGTD23, PH17, PH21, QLH21, RHS+22, RSM+23, RCK+24, RFS20, RHD+23, SMGS22, SWWL23, SJBS21, TML+17a, TML+17b, TML+17c, YXH20, ZHX+22, ZWL+23, ZHL+23, ZNF21, ZZL+22, DL17, HP18, SBJ21, SCM+21, TDPD+21, TCL+21, ZPRD21, ZZW+19, ZG22]. **Hardware-Assisted** [ZHX+22]. **Hardware-In-The-Loop** [OBB+24]. **Hardware/Software** [DLMP21, PH17, RFS20, ZWL+23, HP18]. **Harmful** [PW17b]. **Hart** [USQ+22]. **Hash** [LMP23]. **Hawkbit** [SCL+21]. **Hazard** [DPP22]. **HD** [TBSH22]. **HDL** [BBV+23, LCCS21]. **Healing** [ZZZ+23]. **Heaps** [DG22]. **HeapSafe** [DG22]. **Heterogeneous** [APSH+22, CPG+23, FGD+19, GCL+23, GPV+22, GTP+22, GZK+21, KG22a, RMP+19, VTS+23, WLC22, XZW+22, ZBA+20, WTY+23, EHK20]. **HEVC** [AS18]. **Hidden** [LBDPP19]. **Hierarchical** [BWZ+21]. **Hierarchy** [PKN+20]. **High** [Ano23c, Ano23d, AMG+20, BFP+22, BP21, CXL+20a, DNN23, FHL+22, GRD22, HBSE22, HK20, KZH22, LPZ19, LRB18, MMGC20, MZZG22, MPU+23, PAPJ+23, QCL+23, RLL+21, SJR+23, WLW+21, XYT+22, XYT+23, YXH20, ZZB+20, ZWL+20, ZCH+23, ZXXH22, ZCH22, ZHL+23, DKC+21, KHH22, MS17, WWZL17, WWL+20]. **High-bandwidth** [ZZB+20]. **High-Level** [GRD22, MMGC20]. **High-Performance** [Ano23c, Ano23d, BFP+22, BP21, LRB18, MZZG22, SJR+23, XYT+23, YXH20, ZXXH22, HK20, ZCH22, DKC+21, KHH22]. **High-precision** [ZWL+20]. **High-Quality** [LPZ19]. **High-Speed** [HBSE22, KZH22, RLL+21]. **High-Throughput** [DNN23]. **Highly** [BHT+21, LYZH20, PCW+22, ZSM21]. **Hint** [EGBS22]. **Hint-Based** [EGBS22]. **HIRMA** [SJR+23]. **Hits** [Gen24]. **HL5** [MMGC20]. **HLS** [CWD+21]. **Home** [LXC23, LZH20, Szk21]. **Home-Brew** [Szk21]. **Homomorphic** [AYA+23, PS22a]. **Hoplite** [KG17]. **Horizon** [AAC+23]. **Host** [OBSB23]. **Hot** [Szk21]. **Hotspot** [CPWG23]. **HPC** [OBB+24, PFD21]. **HPCG** [GMFC23]. **HPME** [YXH20]. **HULK** [VTS+23]. **HULK-V** [VTS+23]. **Hummingbird** [SJYZ22]. **Hunting** [RMR21]. **HW** [BDdD19a, KSSMRB23, RPA22]. **HW/SW** [KSSMRB23]. **Hybrid** [HJ23, KG22b]. **Hyperdimensional** [TBSH22]. **HyperSplit** [PLSK20]. **hypervisor** [CLM+22, MP20a, MP20b]. **Hz** [TBK+19].

**I/O** [MRGRCR+21b]. **ICs** [PKC+20]. **Identification** [FAPHD23, HCL+21, KGBH22, MGZ+23]. **identifying** [KSAL21]. **IEEE** [BBdD17, IEE21, IEE22, IEE23, TBL19, KGC+24]. **IEEE-Compliant** [KGC+24]. **II** [AHV+21, COMP19, HVW+21, WAH21]. **ILA** [HZS+19]. **Image** [GAO21, SG23]. **Impact** [Cho18, Cho19, KCGL23, VMO+23, YLT22, WSMRM20]. **Implantable** [AMG+20, GRCRCG+20, MRAM+23]. **Implement** [LCCS21, VOK+22]. **Implementation**

[ABC+20, ASE+21, CTN18, Cil21, FWZL19, FHD22, GAO21, GSDB18, HHB23, HSWM23, HSEKD21, HMTL21, HM21, ISM+23, JSB20, KS22, KKE+22, LHC19, LZH20, LNB+23, MR22, NRA+22, NWP+23, NHML+22, PDLC18, PSZMM21, QLC20, RRJ+21, RSA+23, SJR+23, SUM23, SAF+23, SSB+19, SFGB20, SS22, SNOT20, TS20, TT22, TGT+23, TA22, VMFL23, WSMRM20, WWGW23, WTS21, WYK21, WHB+22, WLC22, YBR+23, YNYD23, YTL+23, YTÖ21, ZGL+21, ZZQ21, DZZZ23, EAI19, GBP21, GG18, KSSMRB23, SCM+21, ZJX20]. **Implementations** [KR24, SJER23, DAK+21]. **Implemented** [CCC+22, FdRES23, EHN23, SMGS22]. **Improved** [LWD20, HK20, JS23]. **Improving** [dAGM23, RAPK23, TLS22, ZZZ+23]. **Imputation** [MRB+23, MRB+24]. **In-Depth** [KNK+21]. **In-Hardware** [HLHK19]. **in-network** [DKC+21]. **In-Order** [SPDLP+22]. **In-System** [WDM22]. **including** [GCL+23]. **Increase** [VKG22]. **IndiRA** [TGT+23]. **induced** [FKS22]. **Industrial** [CXL+20a, YLT+23]. **Industry** [EAI19, LKHK23]. **Inevitable** [RK23]. **Inference** [AEAS21, ADF+23, DFA+23, GTC+21a, GTC+21b, GPV+22, GTP+22, GDR+22, NRB+23, OGT+20, PMBA19, SB23, TTB22, TBSH22, GRC+19]. **Information** [MTAL22, PDLC18, POMD22, SS19, WGZ+23]. **Infrastructure** [ZZB+20]. **infrastructures** [AAC+23]. **ing** [DCM23]. **Injection** [AMRCP21, BWZ+21, DXYZ19, ELG20, JRW+23, KNK+21, LBDPP19, POMD22, WW21]. **Innovating** [CXL+20b]. **Input** [TLB+22]. **Insertion** [LSB22]. **Insights** [SG23]. **Inst** [RZAH+19a]. **Inst/s** [RZAH+19a]. **Instance** [BRH+19]. **instantiation** [DL17]. **Instruction** [AKMS21, AP14, CLW23, DAHK20, DDM+20, DMR+20, FSS20, FHD22, GZC22, GAMG+23, dAGM23, HMJ22, HMJ24, HCZ21, HZS+19, JSB20, JZWL23, JHLD21, JHQ23, JRW+23, KLP+20, KG22c, KGBH22, LPZ19, Liu21, MR22, NDZ+21, NKH+21, Pat17, PPS+19, PMKZ22, QLC20, RHGD21, SNH22, SUAR23, Smi24, TBLD23, WZW+19, WZW+21, WLI23, WWX+24, WA21, WAH21, ZPRD22, ZHC+18, ZHX+22, ZZL+22, Chi23, HYXW22, PKL21, PKKK22, Pat18, RPSD16, WLA+13, ZJX20]. **Instruction-Controlled** [SNH22]. **Instruction-Level** [HZS+19, KLP+20]. **Instruction-Set** [HMJ22]. **Instructions** [BSSW21, CWS+24, GCL+23, KAMS19, KKEG22, LYL23, MMD+22a, NNPG23, PW17b, RZAH+19b, KK21, LSB22, LGB17, PJL21, WWW23]. **Instructions/s** [RZAH+19b]. **Insulin** [YBR+23]. **INT** [SSB22]. **Integer** [ADF+23, PCO+23, PMKZ22]. **Integrate** [MMD+22a]. **Integrated** [GTCS21, KCZ+17, TLB+22, TCH23, WCL23, ZSM21, LZW+15, MSFK21, WRD+17, ZLP+15]. **Integrating** [FHY19]. **Integration** [KFGH+23, VMO+23, ZLC19, ZBA+20, HUL+22]. **Integrity** [DBGJ19, FHL+22, HYML23, TZG+23, TA22, ZPRD23, PKKK22]. **Intel** [CKTK22, CKTK23, NGS20, SNOT20, SNOT21]. **Intelligence** [MST+23, WCGL23]. **Intelligent** [GCL+23, GXLW22, HSR+23, LXC23]. **intended** [SGCGCR17]. **Intensive** [LWC18]. **Inter** [KIS20]. **Inter-Chiplet** [KIS20]. **interaction** [AS24]. **Interconnect** [LLL+21, EHN23]. **Interface** [GTCS21, KIS20, MST+23, NRA+22, OPY+18, PH17, PH21, ZS23, SNM22]. **Interleaved** [BCM+21]. **Interleaved-Multi-Threading** [BCM+21]. **Intermittent** [PPYB23]. **Internal** [SNOT20]. **Internet** [DGA+17, SCR+17]. **Internet-of-Things** [SCR+17]. **Interposer** [PKC+20]. **Interposer-Based** [PKC+20]. **Interpreter** [GVT+22]. **interpreters**

[KKC+16]. **Interrupt** [EHK20, MTCL21]. **Introduction** [Bor23]. **Intrusion** [LXC23]. **Invasive** [TBLD23]. **Investigation** [OCC+17]. **INVITED** [DGH19]. **IO** [NAL22]. **IOT** [ZPRD21, ASE+21, ABP22, ASH19, BHT+21, CTN18, CXLL22, CWS+24, CPG+23, CRP+23, DNKDN+24, FRC+18, GTC+21a, GTC+21b, GST+17, HBSE22, HSR+23, LXC23, MLD+23, gMCP19, NBT22, PDLC18, SRD+21, SSD+21, TSABTM20, ZGL+21]. **IoT-Driven** [gMCP19]. **IP** [BBVB20, Bis21, BGVB18, HHB+19, KHH22, PPS+19, PH18, TL22, WDM22, ZCH22]. **IP-XACT** [PPS+19, PH18]. **IR** [YLT22]. **Irradiation** [SML+22]. **ISA** [AKMS21, AS18, ABP22, AHB20, BPF+22, BBVB20, BP21, BGVB18, Chi23, Chi24, FAPHD23, GTC+20, GBP21, GMK+23, GFB+24, IZG22, KGHRM23, LCN+23, LGB17, LVR+20, MAS18, MB16, PRS+15, SZHB21, SFGB20, TMR+19, TZ22, TBLD23, TEYK21, TYEK21, TML+17a, TML+17b, TML+17c, WA21, WGZ+23, YYP+22, ZTC21]. **ISA-Level** [FAPHD23]. **ISAs** [KRR22]. **ISE** [MPP21]. **Isolation** [CYJ+22, KLP+20]. **Issue** [EGBS22, KSRT23, SZHB21]. **ITUS** [KCHYM19].

**Japan** [TBL19]. **JIT** [DCL23]. **July** [BBdD17]. **June** [IEE21, TBL19].

**Kernel** [GPL22, HYML23, SMOM19, VMFL23]. **Key** [DNKDN+24, MLD+23]. **Keys** [DCEJ21]. **Keystone** [SNOT20, SNOT21]. **kHz** [TBK+19, WBH+18, WBH+19]. **Kid** [SEM19]. **Kitten** [GPL22]. **Klessydra** [CSM+21]. **Klessydra-T** [CSM+21]. **Kyoto** [TBL19].

**LAC** [FSS20]. **Language** [Dos19, Smi24]. **Languages** [WWN23]. **Large** [gMCP19]. **Large-Scaled** [gMCP19]. **Last** [CKTK22, CKTK23]. **Latency** [MLPH23, MST+23, RRC+20, RHD+23]. **Layer** [KYDÖ21, Suv21a, VOK+22]. **Layout** [PGTD23]. **Leakage** [Bis21, PAPJ+23, POMD22, TBK+19, AS24]. **Leakage-Suppression** [TBK+19]. **Learn** [LF22]. **Learning** [AEAS21, FHY19, HSL+23, RRC+20, SLCK21, SSD+22, TBR+22, KMS22, RCMQO24]. **led** [Chi23]. **Left** [AS22]. **LeNet** [FWZL19]. **LeNet-5** [FWZL19]. **Length** [MAS18]. **Level** [CKTK22, CKTK23, DDM+20, FAPHD23, GMS+23, GRD22, HYML23, HJ23, HGJD20, HZS+19, MMGC20, RHGD21, WTZ+20, WGZ+23, YLT22, APHD22, CLM+22, HGPD20, KLP+20, MRGRCR+21b]. **Level-1** [DDM+20]. **Leverage** [FDMM22]. **Leveraging** [RHD+23, KG22c]. **Libraries** [FTRH20]. **Library** [GRC+19, Liu21, SEG20, SNOT20, Ano20]. **License** [LRF+21]. **LiFi** [RSM+23]. **LiFi-CFI** [RSM+23]. **Light** [RSM+23, SLB+22, ZSM20, MMR+17]. **Light-weight** [RSM+23]. **Lightweight** [CRRS22, DBP21, GPL22, GTD+23, GJC23, HYWP+19, KKK+17a, KKK+17b, KKK+17c, LPB+21, LCW+24, MCL+21, MCL22, MLPH23, MLD+23, MÇB22, OBSB23, PHC+23, SZHB21, SMJ21, TBSH22, TGMD20, TGMD21, MPP21, MP20a, MP20b]. **Limitations** [RHS+22]. **line** [RCS+19]. **Linear** [FTRH20, GTD+23, ZGD22]. **LinearUCB** [ABM+23]. **Linux** [CIPR21, DRN+23, ILG19, OBSB23, PS22a, SGP+23, SMOM19, VTS+23, ZB19]. **Linux-Capable** [OBSB23, CIPR21]. **Linux-Ready** [PS22a, ZB19]. **LIRA** [SMJ21]. **LIRA-V** [SMJ21]. **lite** [DRC+16]. **LiteAIR5** [GMS+23]. **little** [Lu21b]. **little-core** [Lu21b]. **LLVM** [RSS+21, RSRT19, WY23]. **LLVM-Based** [RSS+21, RSRT19]. **Lo-RISK** [PAPJ+23].

**Localization** [SJER23]. **Lock** [NKTS23]. **Lock-Step** [NKTS23]. **Lockstep** [SAF+23]. **Logic** [EAI19, HLP+24, TBK+19, AFP+17]. **London** [BBdD17]. **Long** [QLC20, GMFC23, VMFL23]. **long-vector** [GMFC23]. **Look** [SMP22]. **Looking** [HGD20a]. **Loop** [OBB+24, RHD+23]. **Low** [ABP22, BPM+21, BPF+22, BP21, CCA+18a, CCA+18b, DCL23, FGD+19, GRC+19, GZK+21, HWG22, KM21, KSRT23, KMB22, LRF+21, LHT+21, MLPH23, MST+23, MRGRCR+21b, MRAM+23, MDR19, PHC+23, PAPJ+23, RKH+23, RAPK23, RMR21, RHD+23, SG23, SLZ+20, SED+23, SRD+21, SSD+21, SR22, SLCK21, TBR+22, ZCH22, CPL+24, DKC+21, ERGK21, GBP21, NKTS23, PCL+23, SCR+17, VTS+23, ZWL+20]. **Low-Area** [MDR19, SSD+21]. **Low-Cost** [BPM+21, DCL23, RMR21, SG23, SLZ+20, HWG22, RAPK23]. **Low-Latency** [MLPH23, MST+23, RHD+23]. **Low-level** [MRGRCR+21b]. **Low-Overhead** [SR22]. **Low-Power** [GZK+21, KSRT23, LRF+21, LHT+21, MRAM+23, MDR19, PHC+23, SED+23, SRD+21, SSD+21, DKC+21]. **Low-Precision** [BPF+22]. **Low-resource** [ZCH22]. **Low-Voltage** [CCA+18a, CCA+18b]. **LRCN** [LCF23]. **LTE** [WRD+17]. **LTE/Wi** [WRD+17]. **LTE/Wi-Fi** [WRD+17]. **LUT6** [LCG+23]. **LUT6/mm2** [LCG+23]. **LWE** [ZXXH22].

**M** [LWD20]. **M/T** [LWD20]. **Machine** [AEAS21, LCW+24, MST+23, SWW+21, KKC+16, KMS22]. **Main** [ZGG23, GAE+23]. **mainframe** [Pat18]. **Management** [AHB20, EHK20, KCZ+17, PACB21, SAW+20, VOK+22, WSK+20, GG18]. **Manager** [Suv21b, TCH23]. **MANIC** [GAE+23]. **Manipulation** [BSSW21, JSB20, KAMS19]. **Manticore** [ZSB21]. **Manual** [WA21, WAH21]. **Many** [BZVCB23, KHG20, KG22a, OBB+24, Chi23]. **Many-Core** [BZVCB23, KHG20, KG22a, OBB+24]. **Manycore** [GCL+23, KG22b, RZAH+19b, RZAH+19a]. **Mapping** [APSH+22]. **March** [GD19]. **Market** [Gen24, SEM19]. **Marsellus** [CPG+23]. **Massively** [Gra16]. **Matching** [TT22]. **Math** [Liu21]. **Matrix** [SSS+22, TBR+22, ZXXH22, GBP21]. **Matrix-Multiplication** [TBR+22]. **Maximizing** [LMP23]. **McEliece** [PGZMG21]. **McPAT** [ZBZ+23]. **McPAT-Calib** [ZBZ+23]. **MCU** [BPM+21, KKH+20, LRF+21, MGZ+23, YLT+23, YTL+23]. **MCU-Based** [LRF+21]. **MCUs** [BB21, TTB22]. **means** [LPB+21]. **Measurement** [SNOT21]. **Mechanism** [GLS21]. **Mechanisms** [DBGJ20]. **mediated** [GG18]. **Medical** [AMG+20, GRCRCG+20, KM21, MRAM+23]. **meet** [ZPRD21]. **MEG** [ZZB+20]. **Memories** [ZUSK23]. **Memory** [BR24, Cil21, CDW+24, DLMP21, GKB+22, KAR+19, KG22b, KLP+20, MST+23, MDR19, NAL22, RRC+20, RCK+24, SB23, SMOM19, TML+17a, TML+17b, TML+17c, TCH23, YXH20, ZZB+20, ZHLR22, ZHL+23, ZC23, DUM+19, GAE+23, WRD+17]. **memory-based** [WRD+17]. **Memory-Constrained** [ZHLR22]. **Memory-Latency-Accuracy** [RRC+20]. **Memory/Accelerator** [KG22b]. **MemPool** [VMO+23, VMO+22]. **Mesh** [RZAH+19a]. **Metadata** [VOK+22]. **Metamorphic** [RHGD21]. **MetaSys** [VOK+22]. **Metering** [WT19]. **Method** [CLWL21, DDM+20, DLMP21, GZC22, HCZ21, LHT+21, WZW+19, ZZZ+23]. **Methodologies** [DXT+18]. **Methodology** [LLS22, MMA+18, RTRM19, RMR21, XYT+22, XYT+23, Bar20]. **metrics** [GYW+23]. **MHz** [UD18]. **Micro** [BP21, DNKDN+24, GRCRCG+20, KNK+21,

MTAL22, MST+23, DPV+17, RPSD16]. **Micro-Architectural** [MTAL22]. **Micro-Architecture** [BP21, KNK+21]. **Micro-Controller** [DNKDN+24, GRCRCG+20, MST+23]. **Microarchitectural** [BB21, CPWG23, Cho18, Cho19, GWZS23, WSG+21]. **Microarchitecture** [BSZ+21, BSZ+24, LHK23, SVM+23, TSW+23, TAC+22, ZBZ+23]. **Microarchitectures** [KIS22]. **Microcoded** [KG22c]. **Microcontroller** [DWG+20, MDR19, SJR+23, DRC+16, DGA+17, GAE+23, HUL+22, MRGRCR+21a]. **Microcontrollers** [KKE+22, RFS20, MRGRCR+21b]. **Microprocessor** [CTN18, HSL+23, KHS+23, PMKZ22, POMD22, QYZ21, SS22, TBK+19, UD18, UD20, WT19, WCL23, BMM+20, BCM+21]. **Microprocessors** [AMRCP21, LWC+16]. **MicroRV32** [APHD22]. **Microscopy** [SG23]. **MicroTESK** [CKK+18]. **Millimeter** [KKH+20]. **Millimeter-wave** [KKH+20]. **Milliwatts** [RHD+23]. **MiniFloat** [BPF+22]. **MiniFloat-NN** [BPF+22]. **Minimal** [BKS22, JK20]. **Minimally** [TBLD23]. **MINOTAuR** [GCR+23]. **MIPS** [COMP19, MTJ+22]. **MIPS-II** [COMP19]. **Mitigate** [KFK+19]. **Mitigating** [GLS21]. **Mixed** [BRH+19, NRB+23, OGT+20, CIPR21]. **mixed-criticality** [CIPR21]. **Mixed-Precision** [NRB+23, OGT+20]. **Mixed-Signal** [BRH+19]. **ML** [DEA+21, DtEt22, HH23, SJER23]. **ML-Based** [SJER23]. **mm2** [LCG+23, LCG+23]. **Mobile** [KKH+20, USQ+22, ZSM20]. **Mode** [HMJ24]. **Model** [DAKK19, JS23, LCF23, MMA+18, TML+17a, TML+17b, TML+17c, SC17]. **Modeled** [PPS+19]. **Modeling** [GMS+23, PH18, RSRT19, ZBZ+23]. **Models** [GDR+22, TBLD23, TAC+22, TDH+23, KSAL21]. **Modern** [LF22, MP20a, MP20b]. **Modification** [KCGL23]. **Modular** [BPF+22, KAR+19, KHG20]. **Module** [TA22, WTZ+20, DZZZ23, MRGRCR+21b, TDPD+21, ZXXH22]. **Module-LWE** [ZXXH22]. **Modules** [AKMS21]. **Monitoring** [CTSG22, DEC+18, LYZH20, SMB17, ZHX+22]. **Monte** [BFP+22]. **MOPS** [GAE+23]. **MOPS/mW** [GAE+23]. **Morello** [Sew21]. **moreMCU** [SAB22]. **Morpheus** [AHV+21, HVW+21]. **Motorcycle** [ZS23]. **Moving** [DAKK19]. **MPSoC** [EEI+18, LVR+20, MSR+21, NRA+22, NRLH22]. **MPSoCs** [KAR+19, KEAS+18]. **MRAM** [GAE+23, HWJ23, HJ23, ZBA+20]. **MRAM-Based** [HWJ23]. **MS** [DUM+19]. **Multi** [BKS22, BBV+23, BCM+21, CXL+20a, DKT+23, EHK20, GZK+21, HWJ23, HSL+23, HH23, KYDÖ21, KHS+23, LRF+21, OCC+17, PCO+23, PCA+24, PNV22, SGP+23, TH22, VROdlT22, WTY+23]. **Multi-Accelerator** [GZK+21]. **Multi-Armed** [DKT+23]. **Multi-Core** [BBV+23, CXL+20a, EHK20, GZK+21, HWJ23, LRF+21, PCA+24, SGP+23, TH22, WTY+23]. **Multi-Grain** [VROdlT22]. **Multi-Layer** [KYDÖ21]. **Multi-objective** [HH23]. **Multi-Precision** [PCO+23, HSL+23]. **Multi-Target** [KHS+23]. **Multi-tasking** [BKS22]. **Multi-threaded** [OCC+17]. **Multicore** [CDF+20, DAKK19, IK21b, JHL+21, PHC+23, PACB21, PGW+20, VMO+22, VMO+23, FKS22, RCMQO24]. **Multiple** [BDdD19b, FGD+19, KKEG22]. **Multiple-precision** [BDdD19b]. **Multiplication** [CPLS23, ERGK21, KZH22, SSS+22, TBR+22, GBP21]. **Multiplier** [VSD22]. **Multiprecision** [CSZ+20]. **multiPULPly** [ERGK21]. **Multirate**

[BHR+18]. **Multithreaded** [CSM+21, EGBS22]. **Mutation** [FAPHD23, HTGD21]. **Mutation-based** [HTGD21]. **Mutation-Classes** [FAPHD23]. **mW** [GAE+23].

**Nano** [Ben23, KMB22]. **Nano-Drones** [Ben23]. **Nano-UAV** [KMB22]. **Nanosatellite** [RKH+23]. **nanotube** [AFP+17]. **NanoWattch** [TLB+22]. **Native** [MDPM24, WWN23]. **natural** [SGCGCR17]. **Navigation** [KMB22]. **Near** [CKTK23, GST+17, MGZ+23, UD20, WCL23, ZZB+20, CKTK22]. **Near-data** [ZZB+20]. **Near-Sensor** [MGZ+23]. **Near-Threshold** [GST+17, UD20, WCL23]. **NEC** [GMFC23, VMFL23]. **Negative** [HGD20a]. **NEORV32** [BFC+23]. **Network** [ABW+21, CRRS22, GRC+19, KSAL21, LHD+22, LPL22, NRA+22, NBT22, RZAH+19a, SLMS21, DKC+21, HC20, HUL+22, TZ22, WWZL17]. **Networks** [ERGK21, GTC+20, GTC+21a, GTC+21b, NRB+23, RHD+23, Suv21b, CRRS21]. **Neumann** [KFK+19]. **Neural** [ABW+21, CRRS22, ERGK21, GRC+19, GTC+20, GTC+21a, GTC+21b, KSAL21, LPL22, NRB+23, RHD+23, CRRS21, HUL+22, TZ22]. **Neuromorphic** [FSMU21, MST+23, RHD+23]. **Neuron** [NBT22]. **Neutral** [LHD+22]. **Neutron** [BFC+23, CG23, SLK+21, SML+22, WW19, WWB23, FKS22]. **neutron-induced** [FKS22]. **News** [Gen24, Gre20]. **Next** [CSO+23, GD19, Ben23]. **Next-generation** [CSO+23, Ben23]. **Night** [CPL+24]. **Nile** [DEC+18]. **nm** [BRH+19, CSZ+20, CCA+18a, KCZ+17, LCG+23, MSFK21, NWP+23, PCO+23, RZAH+19b, SAW+20, SWW+22, UD18, UD20, WBH+18, WBH+19, WSK+20, WCL23, ZB19, ZLP+16, ZCNA17]. **NN** [BPF+22, GRC+19]. **NoC** [EEI+18, KG17, KEAS+18, NRA+22, PKC+20]. **NoC-Based** [EEI+18, KEAS+18]. **NoC-MPSoC** [NRA+22]. **Node** [CPG+23, RRC+20]. **Nodes** [GTC+21a, GTC+21b, SRD+21]. **NOEL** [And20, SAF+23, dOK23]. **NOEL-V** [And20, SAF+23, dOK23]. **Non** [DDM+20, KGHRM23, MTT21]. **Non-Binary** [KGHRM23]. **Non-Blocking** [DDM+20]. **Non-Volatile** [MTT21]. **Nonlinear** [BKdLSGL23]. **Nonvolatile** [SNH22, ZUSK23]. **Novel** [DDM+20]. **NTT** [KZH22, PS22a]. **NTT-Based** [KZH22]. **Number** [JZWL23, KA20, KRR22, MSSS23, NDZ+21, RKRF21]. **Numerics** [BDdD19a]. **NVDLA** [FHY19, FWZL19]. **NVIDIA** [FHY19]. **NvMISC** [ZUSK23]. **nW** [TBK+19, TLB+22].

**O** [MRGRCR+21b]. **Obfuscation** [WZW+19]. **object** [ZZW+19]. **objective** [HH23]. **obtained** [BCM+21]. **off** [GG18, MTJ+22]. **Offs** [RRC+20, ZHLR22]. **On-Board** [CDF+20, RKH+23, ZSM21]. **On-Chip** [DCM23, GPV+22, GTP+22, OBB+24, RZAH+19a, WSK+20]. **On-line** [RCS+19]. **On-Sensor** [SED+23]. **Onboard** [CGG21, DBP21]. **One** [DNKDN+24, KG22c]. **One-Pass** [DNKDN+24]. **Online** [GKB+22, SJER23]. **Oolong** [MB16]. **Open** [ABC+20, APHD21b, Ano23c, Ben23, BPF+22, BCZ21a, CTN18, CKP19, CSO+23, DXT+18, EMMB19, FTRH20, Gen24, GCCR21, HCW23, HLHK19, HHB+19, ILG19, JHL+21, LNA21, MMD+22b, MMD+22c, MFM+19, NNPG23, PW17a, PFD21, PCW+22, PCO+23, PCA+24, PGW+20, SAF+23, SSR+18, VOK+22, WW21, WSG+21, ZWB19, APHD22, DAK+21, GYW+23, HGTD21, Pat18, SCL+21, TZPL21, TSABTM20]. **Open-Source** [ABC+20, Ano23c, CKP19, DXT+18, FTRH20, Gen24, HLHK19, HHB+19, LNA21, MMD+22b, MMD+22c, PCO+23, PCA+24, PGW+20, SSR+18,

WSG+21, VOK+22, DAK+21, GYW+23, HGTD21, SCL+21, TZPL21]. **OpenASIP** [HMJ22]. **OpenCL** [ETR+20]. **OpenCV** [KSAL21]. **openKylin** [WLY+22]. **OpenLane** [HSEKD21]. **Operable** [TLB+22]. **Operating** [BKS22, GPL22, MSDM23, WSMRM20]. **Operation** [CCA+18b, WCL23]. **operations** [CRRS21]. **Opportunities** [LVPSB+23]. **Optical** [KMB22, PAPJ+23]. **Optimal** [OCC+17]. **Optimisation** [HH23, WWW23]. **optimised** [PJL21]. **Optimization** [BSSW21, BB21, HWJ23, Liu21, Zha22, GMFC23]. **Optimizations** [KCGL23, VOK+22, CLC+20]. **Optimized** [CPLS23, DPP22, KS22, KKE+22, PSS23, PSM23, SLBJ23, CSM22, HUL+22, KK21, MFM+19]. **Optimizing** [LVR+20, TTB22, WWX+24]. **Optimum** [RSA+23, KSAL21]. **Order** [Ano23a, Ant22, CPWG23, CXL+20a, CCA+18a, CCA+18b, DDM+20, GZ22, LHD+21, MFM+19, SGP+23, SSB22, SPDLP+22, ZTC21, PRS+15, RPD+15]. **organisation** [SC17]. **Organization** [LF22, OCC+17, PH17, PH21]. **Oriented** [GVT+22, KGBH22]. **Original** [GTD+23]. **Orthogonal** [WZW+19]. **OSEK** [DL17]. **OSEK-V** [DL17]. **OTA** [SCL+21]. **Out-of-Order** [Ano23a, Ant22, CPWG23, CXL+20a, CCA+18a, CCA+18b, DDM+20, GZ22, LHD+21, MFM+19, SGP+23, SSB22, ZTC21, RPD+15]. **Overhead** [SR22]. **Overlay** [BCCM21]. **Overlays** [VROdlT22]. **Overview** [APHD21a, HHB+19]. **Own** [Szk21].

**P** [CLC+20]. **P870** [Ano23d]. **Pacemaker** [YNYD23]. **Packed** [LYL23, YCL+23]. **Packed-SIMD** [LYL23]. **Packet** [PLSK20, DKC+21, WWZL17]. **Parallel** [GRC+19, Gra16, MAS18, MGZ+23, NRB+23, OBB+24, RCMQO24, ZHL+23, HC20]. **Parallel-Execution-Unit** [MAS18]. **Parallelization** [BZVCB23]. **Parallelizing** [KMB22]. **Partial** [CMV21, CKTG21, WW21]. **Partitioning** [RHS+22]. **Pass** [DNKDN+24, AFP+17]. **Password** [XZW+22]. **patches** [HUL+22]. **Path** [RKRF21]. **Paths** [KRR22]. **Pattern** [TT22]. **Patterns** [MTT21]. **Paving** [BFP+22]. **Payment** [ZSM20]. **PCI** [Lu22]. **PCI-E** [Lu22]. **PCIe** [CRMR+23]. **PCs** [LF22]. **Penetration** [CXLL22]. **Perception** [MST+23]. **Perceptron** [KYDÖ21]. **PERCIVAL** [MMD+22b, MMD+22c, MDPM24]. **Perf** [SNOT21]. **Performance** [AS22, Ano23c, Ano23d, BFP+22, Bis21, BP21, CXL+20a, CTSG22, DDM+20, DRN+23, FHL+22, HGD20b, JBK23, LYZH20, LRB18, MAS18, MZZG22, MPU+23, MÇB22, PAPJ+23, QCL+23, SJR+23, SSS+22, SSB22, SMB17, SNOT20, SNOT21, TZS+21, TLB+22, UD18, VMO+22, VMO+23, WLW+21, XYT+22, XYT+23, YXH20, YLT22, ZB19, ZGMD22, ZGD22, ZCH+23, ZXXH22, CSM22, DKC+21, HK20, JS23, KHH22, MS17, SAB24, TLS22, WWL+20, ZCH22]. **PERI** [TGRK19, TGRK21]. **Periodical** [DWG+20]. **Periodical-Driven** [DWG+20]. **peripheral** [EHN23]. **peRISCVcope** [GVT+22]. **Perspective** [CDP+22, SMP22, AAC+23]. **Petaflop** [SB23]. **Phalanx** [Gra16]. **Photon** [SG23]. **Photovoltaic** [TLB+22]. **Physical** [APHD21b, GKB+22, HYML23, LHK23, MST+23, NWP+23, NAL22, WSUM19]. **Physical-Aware** [LHK23]. **PIC** [SG23]. **PicoRio** [TZPL21]. **PicoRV32** [JBK23]. **Pipeline** [CXL+20a, EGBS22, OCC+17, ZZZ21, GMV20, MG22, YTL+23]. **Pipelined** [DPP22, PMKZ22, PNV22, QCL+23, TGT+23]. **pipelining** [CSM22]. **PIPO** [KS22]. **pJ** [UD18]. **pJ/Cycle** [UD18]. **Plate** [LRF+21]. **Platform** [AKMS20, APHD21b, Ben23, BWP22, BHT+21, CSO+23, EMMB19, GGH+22,

IFO+18, JHL+21, KG22c, LCYK20, LCF23, gMCP19, NGS20, OBSB23, QYZ21, SAB22, WTZ+20, WYK21, WWN23, WMA+21, WMR+22, ZHLR22, ZUSK23, APHD22, DGA+17, FKS22, HGPD20, HGTD21]. **Platforms** [Ano21, MSP23, WWX+24, CIPR21]. **PLL** [RZAH+19b, RZAH+19a]. **Plug** [OBSB23]. **Plug-In** [OBSB23]. **Pluggable** [MC22]. **Pluggy** [MKM20]. **Point** [AVS+22, Ano20, BPM+21, CSZ+20, CPLS23, GFB+24, MSZB19, PSS23, PCO+23, SEG20, ZSB21, ZZQ21, Liu21, PRS+15, YCL+23, YWZL22, ZSB20, ZG22, BDdD19b]. **Pointers** [GM21]. **Points** [JZWL23]. **Poisoning** [AVS+22]. **PolarFire** [DXYZ19]. **Policy** [HWJ23, SSS+22]. **Polynomial** [KZH22, WMGD23]. **popularity** [Chi23]. **Portable** [BCZ21a, LYL23, WHB+22]. **Porting** [GPL22, Zha22]. **Portland** [IEE23]. **Posit** [CLR+21b, CLR+21a, CRRS22, KK23, MSSS23, MMD+22a, MMD+22b, MMD+22c, MDPM24, SJM+20, TGRK19, TGRK21, CRRS21, SJP+23]. **Post** [EKAK22, FSMG+19, FSS20, GJC23, HBSE22, KSFS24, KGHRM23, LKKK22, NDZ+21, PGTD23, PGZMG21, RFS20, TH22, XHY+20, ZKS+23, MRGRCR+21a]. **Post-Layout** [PGTD23]. **Post-Quantum** [EKAK22, FSMG+19, FSS20, GJC23, HBSE22, KSFS24, KGHRM23, LKKK22, PGZMG21, RFS20, XHY+20, ZKS+23]. **Post-Silicon** [TH22, MRGRCR+21a]. **Potential** [LMP23]. **Power** [ABP22, BP21, DHL+21, GRC+19, GZK+21, KM21, KCZ+17, KSRT23, KMB22, LRF+21, LHT+21, MRAM+23, MDR19, OBB+24, PCL+23, PHC+23, PPYB23, SED+23, SRD+21, SAW+20, SSD+21, Smi24, SLCK21, SKK+22, TBR+22, TDH+23, WSK+20, YLT22, ZBZ+23, CPL+24, DKC+21, ERGK21, GBP21, SCR+17, VTS+23, WTY+23, ZWL+20]. **Powered** [TLB+22, AAC+23]. **PPMU** [CTSG22]. **Practical** [MKVD23, VOK+22]. **Precision** [AWB+23, BPF+22, BDdD19a, CRP+23, GFB+24, KGC+24, LCN+23, NRB+23, OGT+20, PCO+23, RSR21, YCL+23, BDdD19b, HSL+23, LWA+14, ZWL+20]. **Precision-Scalable** [CRP+23]. **Predictability** [GCCR21]. **Predictable** [GCR+23]. **Prediction** [BWP22, SLCK21]. **Predictor** [CSM22]. **PRESENT** [TGMD21]. **Preventing** [ARH+22]. **Prevention** [WSG+21]. **PRINCE** [MCL22]. **Principle** [KG22c]. **Printer** [YLT+23]. **Privilege** [TZG+23]. **Privileged** [WAH21]. **Proceedings** [IEE23, GD19, IEE21, IEE22]. **Process** [HMTL21]. **Processing** [AvAG21, ABP22, CCC+19, CGG21, CRRS22, GAO21, HWG22, MSSS23, PCA+24, RMF22, SG23, SED+23, Su21, ZB19, ZZB+20, DKC+21, KHH22, WWZL17]. **Processor** [ABM+23, Ano23a, Ano23c, Ano23d, Ano23g, ABW+20, ABW+21, ADF+23, BBV+23, BZVCB23, BBVB20, BHD23, CCC+22, CDF+20, CSZ+20, CV22, CXL+20a, CLWL21, CKTK22, CKTK23, CPLS23, CCA+18a, CCA+18b, Cho18, Cho19, DAPS21, DDM+20, DPP22, DKT+23, DCC+23, DFA+23, FDS+23, GM21, GZ22, GDR+22, GJC23, GSDB18, HHB23, HCW23, HGJD20, HHB+19, HCZ21, IFO+18, IK21b, JK20, KIS20, KFK+19, KCZ+17, KKOY19, KYDÖ21, KKEG22, KK23, LCCS21, LBDPP19, LHD+21, LHC19, LHT+21, LNA21, LZH20, LLL+21, MLPH23, MSZB19, MMGC20, MFM+19, MAS18, MZZG22, MKB+23, Mis22, gMCP19, NHML+22, NBT22, OCMP19, OCC+17, OGT+20, PSS23, PCL+23, PHC+23, PNSD20, PPS+19, PH18, PCW+22, PCO+23, PCA+24, PSZMM21, PMBA19, PNV22, QCL+23, RKH+23, RHGD21, RZAH+19b, RZAH+19a, RCS+19, SGP+23, SUM23, SLZ+20, SWW+22, SSD+21, SR22, SFGB20, SPDLP+22, SLB+22]. **Processor**

[SLCK21, TS20, TBSH22, TT22, TGT+23, TCH23, VROdlT22, WDM22, WTS21, WMGD23, WW19, WSK+20, XHY+20, ZLC19, ZTC21, ZWB19, ZGL+21, ZGD22, ZGG23, ZXXH22, ZCH22, ZLP+16, ZCNA17, ZC23, dOTB+20, dOK23, AvAG21, AFP+17, BGVB18, CMV21, CPL+24, CSM22, DUM+19, DPV+17, DZZZ23, DAK+21, EHN23, FvHC+23, GAE+23, GMV20, GYW+23, HK20, HYXW22, KK21, KHH22, KMS22, LHD+22, LWA+14, LZW+15, LPB+21, LSB22, MS17, MB16, MMR+17, RPD+15, RPSD16, SJYZ22, YWZL22, ZLP+15, ZCNA16]. **processor-based** [YWZL22]. **processor-micro-architecture** [RPSD16]. **Processors** [AAB+23, BWZ+21, BHT+21, CAL23, CRRS22, DEA+21, DtEt22, DMR+20, FdRES23, FSMG+19, GTC+20, GMK+23, HLHK19, HMJ22, HDT+20, KG22a, KGC+24, KS22, KKE+22, LPZ19, MSP23, MTCL21, MSJ19, OPY+18, OBB+24, PPYB23, RSR21, RTRM19, RMP+19, RMR21, SAW+20, SUAR23, Szk21, WSUM19, WW21, WWB23, XYT+22, XYT+23, YYP+22, ZGMD22, ZCH+23, Bar20, KKC+16, NKTS23, RCMQO24]. **Product** [CXL+20a, KBBA17]. **Prof5** [SCA+22]. **profiler** [SCA+22]. **Program** [CKK+18]. **Programmable** [Ant22, CTSG22, DEC+18, EAI19, HCL+21, Lu22, PLH+22, SAW+20, TSS+22]. **Programming** [BBV+23, Bor23, HLP+24, KGBH22, Smi24, WDM22, WWN23]. **Programs** [WY23, ZPRD23]. **Progress** [HWG22, Liu21]. **Project** [AAC+23]. **Projects** [RBK18]. **Propagated** [LHT+21]. **Properties** [CAL23]. **Proposal** [KKOY19]. **Prospects** [RHS+22]. **protected** [SGCGCR17]. **Protecting** [AHV+21, DGH19, HVW+21, WSUM19]. **Protection** [Bis21, DBGJ20, DCEJ21, GKB+22, HYML23, NAL22, RTRM19, RSM+23, TGMD21]. **Protocol** [DCM23]. **Proton** [dOK23]. **Prototype** [FHD22, HGLD18, ZWL+23, DPV+17, HGPD20]. **Prototypes** [HGLD19, HGTD20, HGD20b, HGTD21]. **Pruned** [MKB+23]. **Public** [MLD+23]. **Public-Key** [MLD+23]. **PUF** [MSFK21]. **PULP** [GRC+19]. **PULP-NN** [GRC+19]. **Pump** [YBR+23]. **purpose** [MRGRCR+21b, TZ22]. **PUSCH** [BZVCB23]. **PVT** [TLS22]. **PWM** [PSM23]. **PYNQ** [SSD+22]. **Pytorch** [KSAL21].

**Q** [Raj21]. **QEMU** [AKMS20, Hor21a]. **Quad** [SR22]. **Quad-Core** [SR22]. **Qualification** [FAPHD23]. **Quality** [LPZ19, SMOM19]. **Quantitative** [ZZZ+23]. **Quantized** [ADF+23, DFA+23, GRC+19, GTC+20, GTC+21a, GTC+21b, NRB+23]. **Quantum** [EKAK22, FSMG+19, FSS20, GJC23, HBSE22, KSFS24, KGHRM23, LKKK22, NDZ+21, PGZMG21, RFS20, XHY+20, ZKS+23]. **Quark** [ADF+23, NWP+23]. **Quire** [MMD+22a, MMD+22b, MMD+22c, SJP+23]. **quire-enabled** [SJP+23].

**race** [SCR+17]. **Radiation** [BFC+23, CG23, SLK+21, WW19, WWB23, dOTB+20]. **Radio** [AHB20, PACB21]. **Radix** [HSE+24]. **Radix-4** [HSE+24]. **RAE** [WWL+20]. **RAM** [DXYZ19]. **Random** [APHD21a, DHL+21, TTB22, TTDD21, LSB22]. **Randomization** [ZZL+22]. **Randomized** [JRW+23]. **Range** [UD18]. **RANTT** [KA20]. **Rapid** [GGH+22, LPZ19]. **RAS** [ZZZ+23]. **Rate** [ZHL+23]. **Rates** [YLC21]. **Raven** [LZW+15]. **Razor** [VKG22]. **Reader** [PW17a]. **Ready** [PS22a, ZB19, CDP+22]. **Real** [APSH+22, BB21, HSWM23, HCL+21, KFGH+23, LHD+21, LHC+21, LCF23, MSDM23, PLH+22, WBH+18, WBH+19, ZHX+22]. **Real-Time**

[HSWM23, KFGH+23, LHD+21, LHC+21, MSDM23, PLH+22, WBH+18, WBH+19, ZHX+22, APSH+22, BB21, HCL+21, LCF23]. **REALISE** [MLD+23]. **REALISE-IoT** [MLD+23]. **Reality** [SED+23]. **Realization** [DNKDN+24, NAL22]. **Reason** [TDPD+21]. **Recognition** [GXLW22, LRF+21, ZWL+20, DZZZ23]. **Recommendation** [DEA+21, DtEt22]. **Reconfigurable** [DAHK20, LYZH20, gMCP19, SR22, Suv21b, VROdlT22, WLI23, ZLC19, SAB22, WRD+17]. **Reconfiguration** [ABM+23, CMV21, CKTG21, WW21]. **reconstruction** [Sah23]. **Recovering** [MTAL22]. **Recovery** [DBP21, XZW+22]. **Recurrence** [HSE+24]. **RedMulE** [TBR+22]. **Reduced** [Pat17]. **Reducing** [MTT21]. **Reduction** [ZCNA17, ZCNA16]. **Redundancy** [ZCNA17, ZCNA16]. **Redundant** [KRR22, RKRF21]. **Reference** [MMA+18]. **Register** [AKMS21]. **Registers** [LBDPP19, MTT21, SZHB21]. **Regression** [ZGD22]. **Regulator** [WCL23]. **Relaxed** [HLP+24]. **Reliability** [AAA+21, AMRCP21, ISM+23, LNZ+22, RAPK23, WSMRM20]. **Reliable** [FSMG+19, MMA+18]. **Remote** [SMJ21, WWL+20]. **Rendering** [TSS+22, ZJX20]. **Replacement** [SSS+22]. **Replication** [DAPS21]. **Reprogrammable** [ZCNA16, ZCNA17]. **Research** [CXLL22, GZ22, GGH+22, HCW23, LPL22, TEYK21, WDM22, APHD22]. **resilience** [BMM+20]. **Resiliency** [CCA+18a]. **Resilient** [CCA+18b, DBP21, NRLH22, WCL23]. **Resisted** [DHL+21]. **Resolution** [WBH+18, WBH+19]. **Resource** [AHB20, ET21, dAGM23, IK21b, JBK23, PACB21, SCL+21, ZCH22]. **Resource-Constrained** [ET21, dAGM23, JBK23]. **Retargeting** [COMP19]. **Retirement** [KKEG22]. **Return** [KGBH22]. **Return-Oriented** [KGBH22]. **Reuse** [ZHL+23]. **Review** [WCGL23, SFAAL22]. **revolutionary** [GG18]. **revolutionize** [Gre20]. **RF** [KKH+20]. **RFID** [IFO+18]. **Rich** [SNOT21]. **RIMI** [KLP+20]. **RISC** [And20, Ano23b, BDdD19b, BFC+23, CKTG21, Cho19, EHK20, KFGH+23, MTAL22, RZAH+19b, TLB+22, WY23, dOK23, ABC+20, AAA+21, ASE+21, AKMS20, AKMS21, AS22, APHD21a, APHD21b, APHD22, APSH+22, AEAS21, AvAG21, AS18, AAC+23, AFP+17, ABP22, AAB+23, AHB20, ABM+23, ARH+22, Ano20, Ano22, Ano23a, Ano23c, Ano23d, Ano23f, Ano23g, Ant22, AMRCP21, AMG+20, AS24, AP14, ABW+20, ABW+21, AWB+23, ADF+23, ASH19, AHV+21, AYA+23, BKS22, BBV+23, BSSW21, BSZ+21, BWZ+21, BSZ+24, BHR+18, BRH+19, BB21, BMM+20, BCM+21, BJN23, Bar20, BFP+22, BKdLSGL23, BCCM21, Ben23, BPM+21, BPF+22, BZVCB23, BBVB20, BP21, Bor23, BPS+23, BWP22, BCZ21a, BCZ21b, BF23, BR24, BHGD21, BHD23, BHT+21, BGVB18, CCC+22, CIPR21, CTN18, CXLL22, CCC+19, CGG21, CG23, CDF+20, CDP+22, CRMR+23, CMV21]. **RISC** [CSZ+20, CV22, CPWG23, CLC+20, CXL+20a, CXL+20b, CWD+21, CLWL21, CKTK22, CYJ+22, CKTK23, CPLS23, CWS+24, Chi23, CCA+18a, CCA+18b, Cho18, CPL+24, CSM22, CAL23, CKK+18, CKP19, COMP19, Cil21, CRRS21, CRRS22, CPG+23, CRP+23, CTSG22, CLW23, CSO+23, DNKDN+24, DAHK20, DHL+21, DNN23, DUM+19, DBP21, DXT+18, DBGJ19, DBGJ20, DG22, DGH19, DAPS21, DCM23, DCEJ21, DYZ+22, DPV+17, DDM+20, DPP22, DKC+21, DKT+23, DZZZ23, DEA+21, DtEt22, DCC+23, DRN+23, DXYZ19, DK23, DAK+21, DKA+22, Dos19, DLMP21, DCL23, DFA+23, DRC+16, DGA+17, DWG+20,

DMR+20, EAI19, EAM+22, EMMB19, EAMK21, EKAK22, EEI+18, ELG20, ETR+20, ET21, EHN23, EGBS22, FSPB21, FDS+23, FHY19, FFW20, FWZL19, FHL+22, FdRES23, FKS22, FTRH20, FGD+19, FRC+18, FvHC+23, FSMU21, FSMG+19, FSS20, FHD22, FAPHD23, FDMM22, GM21, GZ22, GZC22]. **RISC** [GCL+23, GMS+23, GRCRCG+20, GRC+19, GTC+20, GTC+21a, GTC+21b, GPV+22, GTP+22, GGH+22, GBP21, GST+17, GDR+22, GXLW22, GAMG+23, Gen24, GWZS23, GKB+22, dAGM23, GMK+23, GAO21, GG18, GAE+23, GMV20, GMFC23, GGÁARG+21, GZK+21, GPL22, GRD22, GLS21, GTD+23, GVT+22, Gra16, GTCS21, Gre20, GCCR21, GCR+23, GYW+23, GJC23, GSDB18, GFB+24, HYML23, HBSE22, HYWP+19, HWJ23, HJ23, HSR+23, HHB23, HH21, HVW+21, HCP+21, HH22, HK20, HYXW22, HSL+23, HSWM23, HCW23, HLHK19, HMJ22, HMJ24, HGLD18, HGLD19, HGD+19, HGTD20, HGD20a, HGJD20, HGD20b, HGPD20, HGTD21, HTGD21, HSEKD21, HMTL21, HDT+20, HHB+19, HUL+22, HCZ21, HWG22, HH23, HCL+21, HM21, IK21a, IVZV20, ISM+23, ILG19, IFO+18, IK21b, IZG22, JBK23, JSB20, JHL+21, JZWL23, JHLD21, JRD+23, JHQ23, JRW+23, JK20, JS23, KSAL21, KIS20, KIS22, KAR+19, KHG20]. **RISC** [KG22a, KG22b, KK21, KFK+19, KM21, KA20, KFS22, KSFS24, KSSMRB23, KNK+21, KCZ+17, KEAS+18, KKH+20, KLP+20, KS22, KKOY19, KG22c, KRR22, KYDÖ21, KHH22, KAMS19, KGBH22, KHS+23, KMS22, KSRT23, KCGL23, KZH22, KMB22, KKEG22, KCHYM19, KFGH+23, KGHRM23, KK23, KKE+22, LCCS21, LRF+21, LBDPP19, LHD+21, LHD+22, LF22, LWA+14, LZW+15, LWC+16, LCYK20, LPB+21, LHC+21, LKKK22, LCN+23, LKHK23, LYZH20, LWC18, LSB22, LGB17, LHC19, LWD20, LHT+21, LCG+23, LCF23, LMP23, LYL23, LWLA23, LCW+24, LXC23, LVR+20, LNA21, LPZ19, Liu21, LPL22, LHK23, LNZ+22, LLS22, LVPSB+23, LZH20, LLL+21, Lu21b, Lu21a, Lu22, LNB+23, LRB18, MCL+21, MCL22, MLPH23, MSZB19, MKČ23, MKM20, MC22, MSSS23, MMD+22a, MMD+22b, MMD+22c, MSP23, MMGC20, MTCL21, MLD+23, MG22, MR22, MPP21, MFM+19, MTT21, MS17, MAS18, MSJ19, MB16, MST+23, MZZG22, MMR+17]. **RISC** [MSR+21, MSD+22, MSDM23, uhMSI19, MKB+23, MPU+23, MKVD23, Mis22, MGZ+23, MRSBGR+20, MRGRCR+21a, MRGRCR+21b, MRAM+23, gMCP19, MDR19, MTJ+22, MRB+23, MRB+24, MSFK21, MÇB22, MMA+18, NRB+23, NRA+22, NNPG23, NDZ+21, NWP+23, NAL22, NHML+22, NKH+21, NBT22, NGS20, NKTS23, NPA+23, NSM+23, NRLH22, OPY+18, OCMP19, OCC+17, OGT+20, OBSB23, OBB+24, PSS23, PDLC18, PS22a, PLH+22, PKN+20, PKL21, PJL21, PKC+20, PKKK22, PCL+23, PHC+23, PAPJ+23, PGTD23, PRS+15, PNSD20, PW17a, Pat18, PACB21, PPS+19, PH18, PFD21, PCW+22, PCO+23, PGW+20, PMKZ22, PPYB23, PRP+23, PGZMG21, POMD22, PLSK20, PSZMM21, PNG20, PS22b, PSM23, PMBA19, PNV22, QCL+23, QLH21, QYZ21, QLC20, RSR21, RRJ+21, RSR20, RCMQO24, RHS+22, RKH+23, RAPK23, RRC+20, RPD+15, RPSD16, RSA+23, RMF22, RKRF21, RBK18]. **RISC** [RLL+21, RSS+21, RHGD21, RMP+19, RK23, RMR21, RSM+23, RPA22, RZAH+19a, RFS20, RCS+19, RHD+23, SGP+23, SEM19, SMP22, SVM+23, SNM22, SG23, SJR+23, Sah23, SUM23, SNH22, SGCGCR17, SSS+22, SFAAL22, SLZ+20, SLK+21, SML+22, SMMD23, SSB22, SAF+23, SC17, SLBJ23, SBJ21, SMB17, SAB22, SED+23, SCR+17, SSR+18, SRD+21, SAW+20, SWW+21, SWW+22,

SZHB21, SJER23, SSD+21, Sew21, SMGS22, SJM+20, SJP+23, SMJ21, SS19, SWWL23, SR22, SUAR23, SSB+19, SCA+22, SFGB20, Smi24, SB23, SJYZ22, SCM+21, SPDLP+22, SLB+22, SCL+21, SS22, SJBS21, SMOM19, Su20, Su21, SAB24, SNK22, SLCK21, Suv21a, Suv21b, SNOT20, SNOT21, SLMS21, SKK+22, SSD+22, Szk21, TTB22, TS20, TMR+19, TBSH22, TLS22, TT22, TBS+21, TZPL21, TH22, TZS+21, TZ22, TZG+23, TGMD20, TGMD21, TBLD23, TDPD+21, TEYK21, TYEK21]. **RISC** [TSS+22, TGRK19, TGRK21, TGT+23, TAC+22, TSABTM20, TBR+22, TCL+21, TTDD21, TDH+23, TBK+19, TL22, TCH23, TOYK22, TA22, USQ+22, UD18, UD20, VTS+23, VKG22, VROdlT22, VMO+22, VMO+23, VSD22, VMFL23, WSMRM20, WRD+17, WWZL17, WBH+18, WT19, WZW+19, WBH+19, WTZ+20, WZW+21, WLW+21, WLY+22, WDM22, WWGW23, WWW23, WLI23, WWX+24, WTS21, WLA+13, WA21, WAH21, WYK21, WCGL23, WMGD23, WSUM19, WMA+21, WMR+22, WW19, WW21, WWB23, WSG+21, WSK+20, WXY+22, WHB+22, WLC22, WTY+23, WCL23, WGZ+23, XZW+22, XLZ23, XHY+20, XYT+22, XYT+23, YBR+23, YNYD23, Yan20, YLC21, YCL+23, YLT+23, YTL+23, YYM21, YTÖ21, YXH20, YLT22, YWZL22, YYP+22, ZLC19, ZB19, ZSB20, ZSB21, Zee22, ZTC21, ZPRD21, ZPRD22, ZPRD23, ZBZ+23, ZHC+18, ZZW+19, ZWL+20, ZGL+21, ZZG21, ZZZ21, ZGMD22, ZGD22, Zha22, ZHX+22, ZHLR22, ZGG23, ZZZ+23]. **RISC** [ZCH+23, ZXXH22, ZKS+23, ZUSK23, ZZQ21, ZCH22, ZWL+23, ZSM20, ZSM21, ZS23, ZJX20, ZHL+23, ZBA+20, ZLP+15, ZCNA16, ZLP+16, ZCNA17, ZG22, ZPL+23, ZNF21, ZZL+22, ZC23, dOTB+20]. **RISC-HD** [TBSH22]. **RISC-V** [And20, Ano23b, BDdD19b, BFC+23, CKTG21, Cho19, KFGH+23, MTAL22, TLB+22, WY23, dOK23, ABC+20, AAA+21, ASE+21, AKMS20, AKMS21, AS22, APHD21a, APHD21b, APHD22, APSH+22, AEAS21, AvAG21, AS18, AAC+23, AFP+17, ABP22, AAB+23, AHB20, ABM+23, ARH+22, Ano20, Ano22, Ano23a, Ano23c, Ano23d, Ano23f, Ano23g, Ant22, AMRCP21, AMG+20, AS24, AP14, ABW+20, ABW+21, AWB+23, ADF+23, ASH19, AHV+21, AYA+23, BKS22, BBV+23, BSSW21, BSZ+21, BWZ+21, BSZ+24, BHR+18, BRH+19, BB21, BMM+20, BCM+21, BJN23, Bar20, BFP+22, BKdLSGL23, Ben23, BPM+21, BPF+22, BZVCB23, BBVB20, BP21, Bor23, BWP22, BCZ21a, BCZ21b, BF23, BR24, BHGD21, BHD23, BHT+21, BGVB18, CCC+22, CIPR21, CTN18, CXLL22, CCC+19, CGG21, CG23, CDF+20, CDP+22, CRMR+23, CMV21, CSZ+20, CV22, CPWG23, CLC+20]. **RISC-V** [CXL+20a, CXL+20b, CWD+21, CLWL21, CKTK22, CYJ+22, CKTK23, CPLS23, CWS+24, Chi23, CCA+18a, CCA+18b, Cho18, CPL+24, CSM22, CAL23, CKK+18, CKP19, COMP19, Cil21, CRRS21, CRRS22, CPG+23, CRP+23, CTSG22, CLW23, CSO+23, DNKDN+24, DAHK20, DHL+21, DNN23, DUM+19, DBP21, DXT+18, DBGJ19, DBGJ20, DG22, DGH19, DAPS21, DCM23, DCEJ21, DYZ+22, DPV+17, DDM+20, DPP22, DKC+21, DKT+23, DZZZ23, DEA+21, DtEt22, DCC+23, DRN+23, DXYZ19, DK23, DAK+21, DKA+22, Dos19, DLMP21, DCL23, DFA+23, DRC+16, DGA+17, DWG+20, DMR+20, EAI19, EAM+22, EMMB19, EAMK21, EKAK22, EEI+18, ELG20, ETR+20, ET21, EHN23, EGBS22, FSPB21, FDS+23, FHY19, FFW20, FWZL19, FHL+22, FdRES23, FKS22, FTRH20, FGD+19, FRC+18, FvHC+23, FSMU21, FSMG+19, FSS20, FHD22, FAPHD23, FDMM22, GM21, GZ22, GZC22, GCL+23, GMS+23, GRCRCG+20,

GRC+19, GTC+20]. **RISC-V** [GTC+21a, GTC+21b, GPV+22, GTP+22, GST+17, GDR+22, GXLW22, GAMG+23, Gen24, GWZS23, GKB+22, dAGM23, GMK+23, GAO21, GG18, GAE+23, GMV20, GMFC23, GZK+21, GPL22, GRD22, GLS21, GTD+23, GVT+22, Gra16, GTCS21, Gre20, GCCR21, GCR+23, GYW+23, GJC23, GSDB18, GFB+24, HYML23, HBSE22, HYWP+19, HWJ23, HSR+23, HHB23, HH21, HVW+21, HCP+21, HH22, HK20, HYXW22, HSWM23, HCW23, HLHK19, HMJ22, HMJ24, HGLD18, HGLD19, HGD+19, HGTD20, HGD20a, HGJD20, HGD20b, HGPD20, HGTD21, HTGD21, HSEKD21, HMTL21, HDT+20, HHB+19, Hor20, HCZ21, HWG22, HH23, HCL+21, HM21, IK21a, IVZV20, ISM+23, ILG19, IFO+18, IK21b, IZG22, JBK23, JSB20, JHL+21, JZWL23, JHLD21, JRD+23, JHQ23, JRW+23, JK20, JS23, KSAL21, KIS20, KIS22, KAR+19, KHG20, KG22a, KG22b, KK21, KFK+19, KM21, KA20, KFS22, KSFS24, KNK+21]. **RISC-V** [KCZ+17, KEAS+18, KKH+20, KLP+20, KS22, KKOY19, KG22c, KRR22, KYDÖ21, KHH22, KAMS19, KGBH22, KHS+23, KMS22, KSRT23, KCGL23, KZH22, KMB22, KKEG22, KCHYM19, KFGH+23, KGHRM23, KK23, KKE+22, LCCS21, LRF+21, LBDPP19, LHD+21, LHD+22, LF22, LWA+14, LZW+15, LWC+16, LCYK20, LPB+21, LHC+21, LKKK22, LCN+23, LKHK23, LYZH20, LWC18, LSB22, LGB17, LHC19, LWD20, LHT+21, LCG+23, LCF23, LMP23, LYL23, LWLA23, LCW+24, LXC23, LVR+20, LNA21, LPZ19, Liu21, LPL22, LHK23, LNZ+22, LLS22, LVPSB+23, LZH20, LLL+21, Lu21b, Lu21a, Lu22, LNB+23, LRB18, MCL+21, MCL22, MLPH23, MSZB19, MKČ23, MKM20, MC22, MSSS23, MMD+22a, MMD+22b, MMD+22c, MSP23, MMGC20, MTCL21, MLD+23, MG22, MR22, MPP21, MFM+19, MTT21, MS17, MAS18, MSJ19, MB16, MST+23, MZZG22, MMR+17, MSR+21, MSD+22, MSDM23, uhMSI19, MPU+23, MKVD23, Mis22, MGZ+23, MRSBGR+20, MRGRCR+21a]. **RISC-V** [MRGRCR+21b, MRAM+23, gMCP19, MDR19, MTJ+22, MRB+23, MRB+24, MSFK21, MÇB22, MMA+18, NRB+23, NRA+22, NNPG23, NDZ+21, NWP+23, NAL22, NHML+22, NKH+21, NBT22, NGS20, NKTS23, NPA+23, NSM+23, NRLH22, OPY+18, OCMP19, OCC+17, OGT+20, OBSB23, OBB+24, PSS23, PDLC18, PS22a, PLH+22, PKN+20, PKL21, PJL21, PKC+20, PKKK22, PCL+23, PHC+23, PAPJ+23, PGTD23, PNSD20, PW17a, Pat18, PACB21, PPS+19, PH18, PFD21, PCW+22, PGW+20, PMKZ22, PPYB23, PRP+23, PGZMG21, POMD22, PLSK20, PNG20, PS22b, PSM23, PMBA19, PNV22, QCL+23, QLH21, QYZ21, RSR21, RRJ+21, RSR20, RCMQO24, RHS+22, RKH+23, RAPK23, RRC+20, RPD+15, RPSD16, RSA+23, RMF22, RKRF21, RBK18, RSS+21, RHGD21, RMP+19, RK23, RSM+23, RPA22, RZAH+19a, RFS20, RCS+19, RHD+23, SGP+23, SEM19, SMP22, SVM+23, SNM22, SG23]. **RISC-V** [SJR+23, Sah23, SUM23, SNH22, SGCGCR17, SSS+22, SFAAL22, SLZ+20, SLK+21, SML+22, SMMD23, SSB22, SAF+23, SC17, SLBJ23, SBJ21, SMB17, SAB22, SED+23, SCR+17, SSR+18, SRD+21, SAW+20, SWW+21, SWW+22, SZHB21, SJER23, SSD+21, Sew21, SMGS22, SJM+20, SMJ21, SS19, SWWL23, SR22, SUAR23, SSB+19, SCA+22, SFGB20, Smi24, SB23, SJYZ22, SCM+21, SPDLP+22, SLB+22, SCL+21, SS22, SJBS21, SMOM19, Su20, Su21, SAB24, SNK22, SLCK21, Suv21a, SNOT20, SNOT21, SLMS21, SKK+22, SSD+22, Szk21, TTB22, TS20, TMR+19, TBSH22, TLS22, TT22, TBS+21, TZPL21, TH22, TZS+21, TZ22, TZG+23, TGMD20, TGMD21, TBLD23, TDPD+21,

TEYK21, TYEK21, TSS+22, TGRK19, TGRK21, TGT+23, TAC+22, TSABTM20, TCL+21, TTDD21, TDH+23, TBK+19, TL22, TCH23, TOYK22, TA22, USQ+22, UD18, UD20, VTS+23, VROdlT22].
**RISC-V**
[VMO+22, VMO+23, VSD22, VMFL23, WSMRM20, WRD+17, WWZL17, WBH+18, WT19, WZW+19, WBH+19, WTZ+20, WZW+21, WLW+21, WLY+22, WDM22, WWGW23, WWW23, WLI23, WWX+24, WTS21, WLA+13, WA21, WAH21, WYK21, WCGL23, WMGD23, WSUM19, WMA+21, WMR+22, WW19, WW21, WWB23, WSG+21, WSK+20, WXY+22, WHB+22, WLC22, WTY+23, WCL23, WGZ+23, XZW+22, XLZ23, XHY+20, XYT+22, XYT+23, YBR+23, YNYD23, Yan20, YLC21, YCL+23, YLT+23, YTL+23, YYM21, YTÖ21, YXH20, YLT22, YWZL22, YYP+22, ZLC19, ZB19, ZSB20, ZSB21, Zee22, ZTC21, ZPRD21, ZPRD22, ZPRD23, ZBZ+23, ZHC+18, ZZW+19, ZWL+20, ZGL+21, ZZG21, ZZZ21, ZGMD22, ZGD22, Zha22, ZHX+22, ZHLR22, ZGG23, ZZZ+23, ZCH+23, ZXXH22, ZKS+23, ZUSK23, ZZQ21, ZCH22, ZWL+23, ZSM20, ZSM21, ZS23, ZJX20, ZHL+23, ZBA+20, ZLP+15, ZCNA16, ZLP+16, ZCNA17, ZG22, ZPL+23, ZNF21, ZZL+22, ZC23, dOTB+20].
**RISC-V-Based** [HJ23, MKB+23, PCO+23, QLC20, RMR21, TBR+22, BCCM21, GGH+22, GGÁARG+21, HSL+23, HUL+22, KSSMRB23, RLL+21, SJP+23].
**RISC-V/Tensor** [DEA+21, DtEt22].
**RISC-V3** [RKRF21]. **RISC-VTF** [JHLD21]. **RISCV** [ZZB+20, Hor21a].
**RISCV-based** [ZZB+20]. **riscv/QEMU** [Hor21a]. **Rise** [Su20, AYA+23]. **RISK** [PAPJ+23, FFW20]. **Risk-5** [FFW20].
**RLWE** [ZHC+18]. **RNN** [AHB20, CDF+20, PACB21]. **RNN-based** [AHB20, PACB21]. **Road** [BFP+22].
**Roadmap** [FDMM22]. **Robotics** [LCYK20]. **Rocket** [Ano23e, LBDPP19, LNB+23, SBJ21]. **Root** [HSE+24]. **Roots** [Gen24]. **ROS** [LCYK20].
**ROS-Based** [LCYK20]. **rotation** [HC20].
**Routed** [KG17]. **RSA** [KSSMRB23]. **RSM** [TGMD21]. **RTOS** [DL17]. **Running** [GDR+22, IVZV20]. **Runtime** [HGTD20, LWLA23, SAB22, WWN23, WRD+17].
**Runtime-reconfigurable** [SAB22, WRD+17]. **RV** [CKTG21].
**RV-CAP** [CKTG21]. **RV32E** [Ano20].
**RV32I** [DPP22, GRCRCG+20].
**RV32IMAC** [DWG+20]. **RV32X** [WY23].
**RVCoreP** [KK21]. **RVCoreP-32IC** [KK21]. **RvDfi** [FHL+22]. **RVFC** [XLZ23].
**RVfpga** [HCP+21]. **RVNet** [WWZL17].
**RVNoC** [EEI+18]. **RVV** [PCA+24].

**s** [RZAH+19b, RZAH+19a]. **Saber** [KZH22, ZHLR22]. **Safe** [gMCP19]. **SafeLS** [SAF+23]. **Safety** [AAB+23, DLMP21, MKČ23, RLL+21, RCK+24, WMA+21, DUM+19].
**Safety-Critical** [MKČ23, RLL+21, WMA+21]. **SAR** [DRC+16]. **Sargantana** [DCC+23, SPDLP+22]. **SAT** [FSPB21].
**SAT-Based** [FSPB21]. **Satellite** [CDF+20].
**SBST** [FSPB21, FDS+23]. **Scalability** [TH22]. **Scalable** [AKMS20, BZVCB23, CSZ+20, CRP+23, GST+17, KKOY19, PNSD20, RSRT19, TBK+19, WWL+20].
**Scalar** [BDdD19b]. **Scale** [DAKK19, TSW+23, Sew21]. **Scale4Edge** [EAM+22]. **Scaled** [gMCP19]. **Scaling** [DHL+21, LCN+23, TLB+22]. **Scheduled** [QLC20]. **Scheduling** [APSH+22, EGBS22].
**Scheme** [FSS20, LWLA23, WLC22].
**schemes** [HK20]. **Scientific** [BDdD19b, MDPM24]. **Script** [ZNF21].
**Script-Based** [ZNF21]. **Scripting** [KKK+17a, KKK+17b, KKK+17c].
**Sealable** [DCEJ21]. **SealPK** [DCEJ21].
**second** [GCL+23]. **Secure**

[ASE+21, DBP21, FSMG+19, GJC23, HYWP+19, KCHYM19, PDLC18, PKC+20, SSB+19, SS22, SLMS21, ZLC19, BF23]. **Secure-Boot** [HYWP+19]. **Secures** [Gen24]. **Securing** [DG22, PRP+23]. **Security** [AAA+21, AAB+23, Ano22, ASH19, AHV+21, CDP+22, CYJ+22, CAL23, DCL23, FHL+22, GAMG+23, Gen24, GWZS23, HVW+21, NGS20, OPY+18, RRJ+21, SG23, SKK+22, USQ+22, WGZ+23, ZHX+22, ZC23, Lu21a, MMR+17]. **Security-Critical** [SKK+22]. **SEGGER** [Ano20]. **seL4** [DK23]. **Selection** [HSE+24]. **Self** [TLB+22, ZZZ+23]. **Self-Healing** [ZZZ+23]. **Self-Powered** [TLB+22]. **Semantic** [SZHB21]. **Sensing** [DWG+20, EMMB19, TLB+22]. **Sensor** [CGG21, MGZ+23, SED+23, ZS23]. **September** [IEE22, IEE23]. **Sequencing** [WHB+22]. **Sequential** [BBV+23, MTT21]. **Sequrity** [WZW+19]. **Server** [ZZZ+23]. **servers** [LF22]. **services** [BF23]. **Set** [CLW23, DMR+20, FSS20, FHD22, GZC22, dAGM23, HMJ22, HMJ24, HCZ21, JZWL23, JHLD21, KG22c, LPZ19, Liu21, MR22, NDZ+21, Pat17, PMKZ22, Smi24, TBLD23, WA21, WAH21, ZZL+22, EHN23, PKKK22, Pat18, RPSD16, WLA+13, ZJX20]. **Sets** [WZW+19, WWX+24, AP14, Chi23]. **SEU** [DAPS21]. **SGX** [SNOT20, SNOT21]. **SHA** [LMP23]. **SHA-3** [LMP23]. **SHAKTI** [DUM+19, MMR+17]. **SHAKTI-MS** [DUM+19]. **Shakti-T** [MMR+17]. **Shape** [KIS20]. **Shape-Changeable** [KIS20]. **Shared** [IK21b, PHC+23]. **Sharing** [LVR+20]. **shellcoding** [BJN23]. **shift** [HC20]. **SHORE** [DLMP21]. **Short** [KKC+16]. **Short-circuit** [KKC+16]. **Shortcomings** [RHS+22]. **should** [AP14]. **Side** [Bis21, DGH19, HGD20a, JHQ23, LHD+21, AS24, GYW+23]. **Side-Channel** [DGH19, LHD+21, Bis21, AS24, GYW+23]. **SiFive** [Ano21]. **sign** [GG18]. **sign-off** [GG18]. **Signal** [ABP22, BHR+18, BRH+19, CCC+19, RMF22]. **Signature** [GJC23, KSSMRB23]. **Signatures** [KSFS24]. **Signoff** [YLT22]. **SIKE** [EAMK21, EKAK22, RFS20]. **Silicon** [ABC+20, CG23, TH22, MRGRCR+21a]. **SIMD** [AvAG21, LYL23, PKL21, PJL21, PW17b, SPDLP+22, TMR+19, YCL+23]. **Simodense** [PJL21]. **Simplify** [BCCM21]. **Simulation** [AS24, BWP22, CLWL21, DXYZ19, DMR+20, HGTD20, PFD21, SNK22, HGTD21, MG22]. **Simulation-based** [AS24]. **Simulator** [BHT+21]. **Simulators** [IZG22, TBLD23]. **Simultaneous** [ZLP+16]. **Simultaneous-Switching** [ZLP+16]. **Singapore** [GD19]. **Single** [BWZ+21, CLWL21, DPV+17, KFK+19, PCA+24, SZHB21]. **Single-** [PCA+24]. **Single-Issue** [SZHB21]. **Single-Stage** [KFK+19]. **Siracusa** [SED+23]. **Siwa** [GRCRCG+20]. **Size** [BSSW21, LCN+23, SLBJ23]. **Size-Optimized** [SLBJ23]. **Skip** [GAMG+23]. **SLM** [GMK+23]. **Slow** [SCR+17]. **SM2** [CPLS23, SWWL23]. **SM2/3** [CPLS23]. **SM4** [KKE+22, WWGW23]. **Small** [BPM+21, BWP22, TZPL21]. **small-board** [TZPL21]. **SmallFloat** [TMR+19]. **Smart** [CYJ+22, EMMB19, FdRES23, LZH20, SLMS21, YBR+23]. **smartphones** [LF22]. **SMURF** [BDdD19b]. **SNOW** [WYK21]. **SNOW-V** [WYK21]. **SoC** [DEA+21, DtEt22, HZS+19, DBP21, TH22, VMO+23, WTY+23, And20, AMG+20, AYA+23, BHR+18, BRH+19, BFC+23, BGVB18, CPG+23, DHL+21, DCM23, DCC+23, FHY19, FWZL19, FRC+18, GCL+23, GXLW22, GAO21, GZK+21, HSWM23, KCZ+17, LCG+23, Lu21b, MCL22, MLPH23, MSFK21, NWP+23, NGS20, QLH21, RAPK23, SED+23, SRD+21, SSD+21, TBS+21, TSABTM20, TDH+23, TLB+22, TL22, VTS+23, VKG22,

VMO+22, WBH+18, WBH+19, WTZ+20, XZW+22, ZLC19, ZZQ21, ZWL+23, ZSM20, ZSM21, ZS23]. **SoCs** [BWP22, KFGH+23, PGW+20, SAB24, TBR+22]. **Soft** [ARH+22, CMV21, CV22, Cho18, Cho19, DAPS21, FvHC+23, GDR+22, GRD22, KGC+24, KKOY19, LNZ+22, MFM+19, MAS18, OCC+17, PMKZ22, PMBA19, RTRM19, SUAR23, WW19, WWB23, WLC22, ZCH22, dOTB+20, BCM+21, KK21, MS17]. **Soft-Core** [KKOY19, PMBA19, FvHC+23, BCM+21]. **Soft-Cores** [GRD22]. **Soft-Processor** [MAS18, CMV21, MS17]. **Soft-Processors** [SUAR23]. **Softcore** [FdRES23, HLHK19, JBK23, PKL21, PJL21]. **softcores** [TLS22]. **Software** [AHV+21, BB21, Bau17, Bis21, BPS+23, CRMR+23, DAPS21, DYZ+22, DXYZ19, DLMP21, HVW+21, HSL+23, LBDPP19, LKHK23, MSD+22, uhMSI19, PH17, PH21, RFS20, SMGS22, TML+17a, TML+17b, TML+17c, WYK21, ZGMD22, ZGD22, ZWL+23, ZNF21, HP18, MRGRCR+21b, SBJ21, SCM+21, TZPL21, TSABTM20]. **Software-driven** [LKHK23]. **software-emulated** [MRGRCR+21b]. **Software-Hardware** [uhMSI19]. **Software-implemented** [SMGS22]. **software/hardware** [SCM+21]. **SOI** [CSZ+20, KCZ+17, MSZB19, SAW+20, SPDLP+22, WSK+20]. **solution** [CIPR21, KSAL21]. **Solutions** [BWP22]. **SonicBOOM** [LHK23]. **sound** [SGCGCR17]. **sounds** [FvHC+23]. **Source** [ABC+20, APHD21b, Ano21, Ano23c, CTN18, CKP19, DXT+18, FTRH20, Gen24, GCCR21, HCW23, HLHK19, HHB+19, ILG19, LNA21, MMD+22b, MMD+22c, MFM+19, PFD21, PCW+22, PCO+23, PCA+24, PGW+20, SAF+23, SSR+18, WW21, WSG+21, APHD22, DAK+21, GYW+23, HGTD21, SNM22, SCL+21, TZPL21, VOK+22]. **Space** [And20, BSZ+21, BSZ+24, CDP+22, FDMM22, LHK23, RAPK23, SVM+23, SLZ+20, SMMD23, SLBJ23, WLW+21, WMA+21, WMR+22]. **Space-Grade** [WMA+21, WMR+22]. **SpaceFibre** [Suv21b]. **Spaceflight** [MSP23]. **Sparq** [DFA+23]. **Sparse** [WBH+18, WBH+19]. **SPEC** [SSB22, TZS+21]. **Specific** [GGÁARG+21, HMJ22, OBSB23, WT19, XHY+20, YYP+22, ZXXH22, DL17, HP18, LPB+21, Pat18]. **Specification** [CTSG22, HZS+19]. **Specifications** [LPZ19]. **SpecTerminator** [JHQ23]. **Spectral** [WBH+18, WBH+19]. **Spectre** [LHD+22]. **Spectrophotometer** [SLB+22]. **Speculative** [GRD22, GCCR21, GCR+23, JHQ23, VKG22]. **speech** [DZZZ23]. **Speed** [BSSW21, HBSE22, KZH22, LWD20, NDZ+21, RLL+21, ZNF21]. **Speed-Up** [NDZ+21, ZNF21]. **speedAI240** [SB23]. **Speeding** [LMP23, MGZ+23]. **Spike** [Hor21b]. **sprung** [Gen24]. **SQRT** [LGB17]. **Square** [HSE+24, TS20, WTS21]. **SRAM** [FvHC+23, RTRM19, SG23, VKG22, WW19, WW21, WWB23, ZHL+23, ZCNA17, dOTB+20]. **SRAM-Based** [RTRM19, WWB23, ZCNA17, dOTB+20, WW19, WW21]. **Stage** [CXL+20a, GZ22, KFK+19, PMKZ22, CSM22, YTL+23, ZZZ21]. **Standard** [LKHK23, BF23]. **standards** [HC20]. **Started** [Hor20]. **States** [IEE23]. **Static** [LWLA23, RHS+22]. **steady** [SCR+17]. **Stealthy** [PGTD23]. **Step** [NKTS23]. **Stimulus** [AMG+20]. **Storage** [GCL+23, Lu21b]. **Strategies** [PPYB23]. **Strategy** [HJ23]. **Stream** [SZHB21]. **Structurally** [MKB+23]. **Structurally-Pruned** [MKB+23]. **Structure** [LPL22]. **Structured** [ZCH+23]. **STT** [ZBA+20]. **STT-MRAM** [ZBA+20]. **studies** [GYW+23]. **Study** [APSH+22, BHD23, CPWG23, DCM23, HGLD19, HGJD20, PKC+20, PGTD23,

RHGD21, SSB22, SSR+18, WMGD23, YLC21, SCM+21]. **Sub** [ADF+23, DFA+23, UD18]. **Sub-Byte** [ADF+23, DFA+23]. **Submicrosecond** [KCZ+17]. **Suitability** [KRR22]. **Suitable** [SUM23]. **Suite** [CKP19, GYW+23]. **Superscalar** [Ant22, GMV20]. **Superscaler** [DDM+20]. **Support** [BPM+21, CSZ+20, Cil21, KKK+17a, KKK+17b, KKK+17c, KKEG22, MSD+22, PCO+23, WY23, ZG22]. **Supported** [LCN+23, Ano20]. **Supporting** [DRN+23, MZZG22, KK21]. **Supports** [KGC+24]. **Suppression** [TBK+19]. **surveillance** [SGCGCR17]. **Survey** [AAB+23, BR24, CLW23, ET21, IZG22, MSD+22, NGS20, DAK+21, Lu21a]. **Sustainable** [SAB22]. **SVE** [CRRS21]. **SW** [KSSMRB23, MSZB19]. **SweRV** [Ano23f]. **Switched** [ZLP+16, LZW+15, MSFK21, ZLP+15]. **Switched-Capacitor** [ZLP+16, LZW+15, MSFK21, ZLP+15]. **Switching** [HGTD20, ZLP+16]. **SWUpdate** [SCL+21]. **SX** [GMFC23, VMFL23]. **SX-Aurora** [GMFC23, VMFL23]. **Symbolic** [BHD23, TZG+23]. **Symposium** [BBdD17, IEE21, IEE22, IEE23, TBL19]. **Synchronization** [DAKK19]. **Synthesis** [GRD22, MMGC20, NSM+23]. **Synthesizable** [LCG+23, RZAH+19b]. **Synthesized** [RZAH+19a]. **System** [Ano22, BKS22, BWZ+21, GMS+23, GAO21, GPL22, HWJ23, HWG22, ILG19, JS23, KAR+19, KM21, LRF+21, LHD+21, LCF23, LXC23, LZH20, Lu22, MSSS23, MTCL21, MLD+23, MSDM23, Mis22, MGZ+23, NBT22, NRLH22, RLL+21, RHD+23, SMB17, SAW+20, TDPD+21, VOK+22, WSMRM20, WTZ+20, WDM22, WGZ+23, YLT+23, YLT22, ZPRD22, ZZB+20, ZSM21, ZBA+20, ZC23, DGA+17, GG18, HGPD20, SJYZ22, WWZL17, ZZW+19, CKTG21, CYJ+22, CRP+23, DNN23, HYWP+19, HZS+19, KSSMRB23, KCHYM19, MSDM23, NKH+21, RSR20, SLK+21, SML+22, SMMD23, ZNF21]. **System-Aware** [SMB17]. **System-Level** [GMS+23, HGPD20]. **system-on-chip** [DGA+17, CKTG21, CYJ+22, CRP+23, DNN23, HYWP+19, HZS+19, KSSMRB23, KCHYM19, MSDM23, NKH+21, RSR20, SLK+21, SML+22, SMMD23, ZNF21]. **Systematic** [HGD+19]. **Systems** [APHD21b, APSH+22, dAGM23, HJ23, JK20, KG22b, KLP+20, KRR22, KSRT23, LNA21, MKČ23, NAL22, RKRF21, RCS+19, SMP22, SLZ+20, SAB22, WMA+21, ZHX+22, SFAAL22, TCL+21, ZG22].

**T** [CSM+21, LWD20, MMR+17]. **Table** [AS22]. **TAIGA** [MS17]. **TailoredCore** [GGÁARG+21]. **Target** [KHS+23]. **Targeted** [HCP+21]. **Targeting** [And20, BWZ+21, KSRT23, FTRH20]. **Task** [APSH+22]. **tasking** [BKS22]. **TCP** [TL22]. **TCP/IP** [TL22]. **Teaching** [GVT+22, ZTC21]. **Teaching-Oriented** [GVT+22]. **Tech** [Szk21]. **Technique** [POMD22]. **Techniques** [CCA+18a, dOK23]. **Technology** [CCC+22, DCC+23, GG18, ZB19]. **TEE** [SNOT20, YXH20]. **Telemetry** [CDF+20]. **TeleVM** [LCW+24]. **Temperature** [TLB+22]. **Tensor** [DEA+21, DtEt22]. **Teraflops/W** [SB23]. **Tesla** [TSW+23]. **Test** [AAA+21, CKK+18, DKT+23, MKM20, TH22, TTDD21]. **Testability** [AAB+23]. **Testing** [AAC+23, BHGD21, CXLL22, HGLD19, HGD20a, HGJD20, HTGD21, JRW+23, RHGD21, RCS+19, SML+22, WW19, WWB23, dOK23, MRGRCR+21a]. **Tests** [BFC+23, TZS+21]. **Textbook** [HH21]. **their** [WSG+21]. **Theoretic** [KA20, NDZ+21]. **Thermal** [OBB+24, VMO+22, VMO+23]. **Things** [DGA+17, SCR+17]. **Thousand** [DEA+21].

**threaded** [OCC+17]. **Threading** [BCM+21]. **Three** [ZZZ21]. **Three-stage** [ZZZ21]. **Threshold** [GST+17, UD20, WCL23]. **Throughput** [DNN23, VKG22]. **Thwarting** [BR24]. **Tiered** [DXT+18]. **Tightly** [CMV21, GKB+22, GTCS21, ZLP+15]. **Tightly-Coupled** [GKB+22, CMV21]. **tightly-integrated** [ZLP+15]. **TIGRA** [GTCS21]. **Tile** [KG22a, KG22b]. **Tile-Based** [KG22a]. **Tiles** [GCL+23]. **Time** [HSWM23, IZG22, KFGH+23, LHD+21, LHC+21, MSDM23, NNPG23, PLH+22, WBH+18, WBH+19, ZHX+22, ZHLR22, APSH+22, BB21, HCL+21, LCF23]. **Time-Memory** [ZHLR22]. **Time-Triggered** [NNPG23]. **Timer** [EHK20]. **Timescales** [KCZ+17]. **Timing** [Bis21, BWP22, GCCR21, GCR+23, LHT+21, NNPG23, UD20, VKG22, WSG+21]. **Timing-Instructions** [NNPG23]. **Tiny** [GVT+22, NBT22, BPM+21]. **Tiny-FPU** [BPM+21]. **Tissue** [AMG+20]. **TL** [MKVD23]. **TL-Verilog** [MKVD23]. **TLB** [PKN+20]. **TMR** [WW21, WWB23]. **Tolerance** [DKA+22, RMP+19, SMGS22, JS23]. **Tolerant** [BCM+21, SLZ+20, SML+22, SMMD23, SR22, SUAR23, VSD22, WW19, dOK23]. **Tool** [AMRCP21, PFD21, RBK18, MG22, Sah23, SCA+22]. **Toolchain** [TZS+21]. **Tools** [DRN+23, MSJ19]. **Toolset** [HMJ22]. **TOPS** [NRB+23]. **TOPS/W** [NRB+23]. **Torus** [KG17]. **Tournament** [CSM22]. **TPM** [BCZ21b, SJBS21]. **TPU** [Pat18]. **Trace** [HWG22, KGBH22, KKEG22, ZPRD22]. **tracing** [BPS+23]. **Tracking** [PDLC18, SS19, WGZ+23]. **Trade** [MTJ+22, RRC+20, ZHLR22]. **Trade-off** [MTJ+22]. **Trade-Offs** [RRC+20, ZHLR22]. **traffic** [SJYZ22]. **Training** [BPF+22, GPV+22, GTP+22, LCN+23]. **Transactions** [SLMS21]. **Transceivers** [KKH+20]. **Transducers** [FdRES23]. **Transform** [KA20, NDZ+21]. **Transformer** [JHLD21]. **Transformers** [MKB+23]. **Transient** [YLC21]. **transistor** [AFP+17]. **Transition** [TZG+23, TDH+23]. **translation** [TOYK22]. **Translator** [RSS+21]. **Transmission** [Suv21b]. **Transparently** [LKHK23]. **Transport** [Suv21a]. **Transprecision** [MSZB19]. **TriCheck** [TML+17a, TML+17b, TML+17c]. **Triggered** [NNPG23]. **Trigonometric** [GZC22, NKH+21]. **Triple** [HJ23]. **Triple-Level** [HJ23]. **Trisection** [TML+17a, TML+17b, TML+17c]. **Trojan** [DCM23, PGTD23]. **Trojan-D2** [PGTD23]. **Trojan-ing** [DCM23]. **Trojans** [ARH+22, DCM23, PGTD23]. **True** [ZNF21]. **Trust** [SJBS21]. **Trusted** [AVS+22, BCZ21a, CDW+24, HDT+20, MCL+21, SNOT21, USQ+22]. **TrustZone** [SNOT21]. **try** [Chi23]. **TS** [SNOT21]. **TS-Perf** [SNOT21]. **tuning** [YCL+23]. **Turna** [Sah23]. **Tutorial** [Ano22, GG18]. **TVM** [CLC+20, YCL+23]. **Type** [BDdD19a, KK23]. **Typed** [KKK+17a, KKK+17b, KKK+17c].

**UAV** [KMB22]. **UEFI** [Zha22]. **UK** [BBdD17]. **Ultra** [ABP22, ERGK21, GRC+19, KMB22, PCL+23, TBR+22, VTS+23, ZSB20, ZWL+20, CPL+24, SCR+17]. **Ultra-efficient** [ZSB20]. **Ultra-Low** [ABP22, KMB22, PCL+23, CPL+24]. **Ultra-Low-Power** [TBR+22, ERGK21, VTS+23, ZWL+20, SCR+17]. **Ultraefficient** [ZSB21]. **Ultralow** [PPYB23]. **Ultralow-Power** [PPYB23]. **UltraScale** [dOK23, SFGB20]. **Undergraduates** [MSJ19]. **Unified** [HSE+24]. **Uniform** [HZS+19]. **Unifying**

[EHK20]. **Unit** [AVS+22, AvAG21, BPF+22, CRRS22, CTSG22, GKB+22, ISM+23, LYZH20, MSZB19, MC22, MSSS23, MAS18, MST+23, PS22b, QCL+23, SMB17, ZHX+22, ZSM21, EHN23]. **United** [IEE23]. **Universal** [LLS22]. **Unlock** [Smi24]. **Unprivileged** [WA21]. **Unprotected** [DG22, FvHC+23]. **Unum** [BDdD19b, BDdD19a]. **Updates** [SCL+21]. **Upsets** [BWZ+21]. **Usage** [LVR+20]. **Use** [MDPM24, Szk21]. **user** [CLM+22]. **user-level** [CLM+22]. **Using** [BDdD19a, DAKK19, FSMU21, GJC23, HCP+21, IFO+18, JZWL23, KKH+20, KGBH22, KFGH+23, KK23, LYL23, MSSS23, MAS18, POMD22, RSA+23, RMF22, SLMS21, TBK+19, VKG22, WWX+24, XYT+22, XYT+23, ZZB+20, AFP+17, BPS+23, BHD23, CSM22, GG18, GLS21, HGD20b, JSB20, JRW+23, KSAL21, LCCS21, LLS22, MKM20, PLSK20, SFGB20, SSD+22, WW21, ZGD22]. **Utilization** [SZHB21, ZHL+23]. **Utilizing** [JHL+21, MTT21]. **UVM** [LLS22, BMM+20, CWD+21, WTZ+20].

**V** [And20, Ano23b, BDdD19b, BFC+23, CKTG21, Cho19, EHK20, GBP21, KFGH+23, MTAL22, PRS+15, PCW+22, TLB+22, VKG22, WY23, dOK23, ABC+20, AAA+21, ASE+21, AKMS20, AKMS21, AS22, APHD21a, APHD21b, APHD22, APSH+22, AEAS21, AvAG21, AS18, AAC+23, AFP+17, ABP22, AAB+23, And20, AHB20, ABM+23, ARH+22, Ano20, Ano22, Ano23a, Ano23c, Ano23d, Ano23f, Ano23g, Ant22, AMRCP21, AMG+20, AS24, AP14, ABW+20, ABW+21, AWB+23, ADF+23, ASH19, AHV+21, AYA+23, BKS22, BBV+23, BSSW21, BSZ+21, BWZ+21, BSZ+24, BHR+18, BRH+19, BB21, BMM+20, BCM+21, BJN23, Bar20, BFP+22, BKdLSGL23, BCCM21, Ben23, BPM+21, BPF+22, BZVCB23, BBVB20, BP21, Bor23, BPS+23, BWP22, BCZ21a, BCZ21b, BF23, BR24, BHGD21, BHD23, BHT+21, BGVB18, CCC+22, CIPR21, CTN18, CXLL22, CCC+19, CGG21, CG23, CDF+20]. **V** [CDP+22, CRMR+23, CMV21, CSZ+20, CV22, CPWG23, CLC+20, CXL+20a, CXL+20b, CWD+21, CLWL21, CKTK22, CYJ+22, CKTK23, CPLS23, CWS+24, Chi23, CCA+18a, CCA+18b, Cho18, CPL+24, CSM22, CAL23, CKK+18, CKP19, COMP19, Cil21, CRRS21, CRRS22, CPG+23, CRP+23, CTSG22, CLW23, CSO+23, DNKDN+24, DAHK20, DHL+21, DNN23, DUM+19, DBP21, DXT+18, DBGJ19, DBGJ20, DG22, DGH19, DAPS21, DCM23, DCEJ21, DYZ+22, DPV+17, DDM+20, DPP22, DKC+21, DL17, DKT+23, DZZZ23, DCC+23, DRN+23, DXYZ19, DK23, DAK+21, DKA+22, Dos19, DLMP21, DCL23, DFA+23, DRC+16, DGA+17, DWG+20, DMR+20, EAI19, EAM+22, EMMB19, EAMK21, EKAK22, EEI+18, ELG20, ETR+20, ET21, EHN23, EGBS22, FSPB21, FDS+23, FHY19, FFW20, FWZL19, FHL+22, FdRES23, FKS22, FTRH20, FGD+19, FRC+18, FvHC+23, FSMU21, FSMG+19, FSS20, FHD22, FAPHD23, FDMM22]. **V** [GM21, GZ22, GZC22, GCL+23, GMS+23, GRCRCG+20, GRC+19, GTC+20, GTC+21a, GTC+21b, GPV+22, GTP+22, GGH+22, GST+17, GDR+22, GXLW22, GAMG+23, Gen24, GWZS23, GKB+22, dAGM23, GMK+23, GAO21, GG18, GAE+23, GMV20, GMFC23, GGÁARG+21, GZK+21, GPL22, GRD22, GLS21, GTD+23, GVT+22, Gra16, GTCS21, Gre20, GCCR21, GCR+23, GYW+23, GJC23, GSDB18, GFB+24, HYML23, HBSE22, HYWP+19, HWJ23, HJ23, HSR+23, HHB23, HH21, HVW+21, HCP+21, HH22, HHTo23, HK20, HYXW22, HSL+23, HSWM23, HCW23, HLHK19, HMJ22, HMJ24, HGLD18, HGLD19, HGD+19, HGTD20, HGD20a,

HGJD20, HGD20b, HGPD20, HGTD21, HTGD21, HSEKD21, HMTL21, HDT+20, HHB+19, Hor20, HUL+22, HCZ21, HWG22, HH23, HCL+21, HM21, IK21a, IVZV20, ISM+23, ILG19, IFO+18, IK21b, IZG22, JBK23, JSB20, JHL+21, JZWL23, JHLD21, JRD+23, JHQ23, JRW+23, JK20, JS23, KSAL21, KIS20]. **V** [KIS22, KAR+19, KHG20, KG22a, KG22b, KK21, KFK+19, KM21, KA20, KFS22, KSFS24, KSSMRB23, KNK+21, KCZ+17, KEAS+18, KKH+20, KLP+20, KS22, KKOY19, KG22c, KRR22, KYDÖ21, KHH22, KAMS19, KGBH22, KHS+23, KMS22, KSRT23, KCGL23, KZH22, KMB22, KKEG22, KCHYM19, KFGH+23, KGHRM23, KK23, KKE+22, LCCS21, LRF+21, LBDPP19, LHD+21, LHD+22, LF22, LWA+14, LZW+15, LWC+16, LCYK20, LPB+21, LHC+21, LKKK22, LCN+23, LKHK23, LYZH20, LWC18, LSB22, LGB17, LHC19, LWD20, LHT+21, LCG+23, LCF23, LMP23, LYL23, LWLA23, LCW+24, LXC23, LVR+20, LNA21, LPZ19, Liu21, LPL22, LHK23, LNZ+22, LLS22, LVPSB+23, LZH20, LLL+21, Lu21b, Lu21a, Lu22, LNB+23, LRB18, MCL+21, MCL22, MLPH23, MSZB19, MKČ23, MKM20, MC22, MSSS23, MMD+22a, MMD+22b, MMD+22c, MSP23, MMGC20, MTCL21, MLD+23, MG22, MR22, MPP21, MFM+19, MTT21, MS17, MAS18, MSJ19]. **V** [MB16, MST+23, MZZG22, MMR+17, MSR+21, MSD+22, MSDM23, uhMSI19, MKB+23, MPU+23, MKVD23, Mis22, MGZ+23, MRSBGR+20, MRGRCR+21a, MRGRCR+21b, MRAM+23, gMCP19, MDR19, MTJ+22, MRB+23, MRB+24, MSFK21, MÇB22, MMA+18, NRB+23, NRA+22, NNPG23, NDZ+21, NWP+23, NAL22, NHML+22, NKH+21, NBT22, NGS20, NKTS23, NPA+23, NSM+23, NRLH22, OPY+18, OCMP19, OCC+17, OGT+20, OBSB23, OBB+24, PSS23, PDLC18, PS22a, PLH+22, PKN+20, PKL21, PJL21, PKC+20, PKKK22, PCL+23, PHC+23, PAPJ+23, PGTD23, PNSD20, PW17a, Pat18, PACB21, PPS+19, PH18, PFD21, PCW+22, PCO+23, PGW+20, PMKZ22, PPYB23, PRP+23, PGZMG21, POMD22, PLSK20, PSZMM21, PNG20, PS22b, PSM23, PMBA19, PNV22, QCL+23, QLH21, QYZ21, QLC20, RSR21, RRJ+21, RSR20, RCMQO24, RHS+22, RKH+23, RAPK23, RRC+20, RPD+15, RPSD16, RSA+23, RMF22]. **V** [RKRF21, RBK18, RLL+21, RSS+21, RHGD21, RMP+19, RK23, RMR21, RSM+23, RPA22, RZAH+19b, RZAH+19a, RFS20, RCS+19, RHD+23, SGP+23, SEM19, SMP22, SVM+23, SNM22, SG23, SJR+23, Sah23, SUM23, SNH22, SGCGCR17, SSS+22, SFAAL22, SLZ+20, SLK+21, SML+22, SMMD23, SSB22, SAF+23, SC17, SLBJ23, SBJ21, SMB17, SAB22, SED+23, SCR+17, SSR+18, SRD+21, SAW+20, SWW+21, SWW+22, SZHB21, SJER23, SSD+21, Sew21, SMGS22, SJM+20, SJP+23, SMJ21, SS19, SWWL23, SR22, SUAR23, SSB+19, SCA+22, SFGB20, Smi24, SB23, SJYZ22, SCM+21, SPDLP+22, SLB+22, SCL+21, SS22, SJBS21, SMOM19, Su20, Su21, SAB24, SNK22, SLCK21, Suv21a, Suv21b, SNOT20, SNOT21, SLMS21, SKK+22, SSD+22, Szk21, TTB22, TS20, TMR+19, TBSH22, TLS22, TT22, TBS+21, TZPL21, TH22, TZS+21, TZ22, TZG+23, TGMD20, TGMD21]. **V** [TBLD23, TDPD+21, TEYK21, TYEK21, TSS+22, TGRK19, TGRK21, TGT+23, TAC+22, TSABTM20, TBR+22, TCL+21, TTDD21, TDH+23, TBK+19, TL22, TCH23, TOYK22, TA22, USQ+22, UD18, UD20, VTS+23, VROdlT22, VMO+22, VMO+23, VSD22, VMFL23, WSMRM20, WRD+17, WWZL17, WBH+18, WT19, WZW+19, WBH+19, WTZ+20, WZW+21, WLW+21, WLY+22, WDM22, WWGW23, WWW23, WLI23, WWX+24, WTS21, WLA+13, WA21, WAH21, WYK21, WCGL23,

WMGD23, WSUM19, WMA+21, WMR+22, WW19, WW21, WWB23, WSG+21, WSK+20, WXY+22, WHB+22, WLC22, WTY+23, WCL23, WGZ+23, XZW+22, XLZ23, XHY+20, XYT+22, XYT+23, YBR+23, YNYD23, Yan20, YLC21, YCL+23, YLT+23, YTL+23, YYM21, YTÖ21, YXH20, YLT22, YWZL22, YYP+22, ZLC19, ZB19, ZSB20, ZSB21, Zee22, ZTC21, ZPRD21, ZPRD22, ZPRD23, ZBZ+23, ZHC+18, ZZW+19, ZWL+20, ZGL+21, ZZG21, ZZZ21, ZGMD22, ZGD22, Zha22, ZHX+22]. **V** [ZHLR22, ZGG23, ZZZ+23, ZCH+23, ZXXH22, ZKS+23, ZUSK23, ZZQ21, ZCH22, ZWL+23, ZSM20, ZSM21, ZS23, ZJX20, ZHL+23, ZBA+20, ZLP+15, ZCNA16, ZLP+16, ZCNA17, ZG22, ZPL+23, ZNF21, ZZL+22, ZC23, dOTB+20, dOK23]. **V/Tensor** [DEA+21, DtEt22]. **V1** [Ano23g]. **V3** [RKRF21]. **Validating** [NSM+23]. **Validation** [AAC+23, CKP19, TH22]. **Value** [TBS+21]. **variability** [TLS22]. **Variable** [BDdD19a, GFB+24, MAS18, RSR21, YTL+23]. **Variable-Length** [MAS18]. **Variable-Precision** [BDdD19a]. **variant** [Ano20]. **Vector** [AEAS21, AvAG21, ADF+23, BKdLSGL23, CCC+22, CSZ+20, CV22, CSM+21, CXL+20a, DFA+23, ISM+23, JRD+23, JK20, KKOY19, KZH22, KFGH+23, LMP23, LPL22, MC22, MKB+23, MPU+23, PNSD20, PCW+22, PCO+23, PCA+24, PGZMG21, RSR21, RMF22, SAW+20, SWW+21, SWW+22, SPDLP+22, Su21, WSK+20, XHY+20, ZHC+18, ZKS+23, ZLP+16, GAE+23, GMFC23, KMS22, LWA+14, LZW+15, SCM+21, VMFL23, WWW23, ZLP+15]. **vector-dataflow** [GAE+23]. **Vector-Instruction** [ZHC+18]. **Vectorized** [BKdLSGL23]. **Vectorizing** [CRRS21]. **Vehicles** [CRMR+23, Ben23]. **Verification** [ASE+21, APHD21a, AAC+23, BHD23, CAL23, DDM+20, DKT+23, DMR+20, FAPHD23, GM21, HGJD20, HZS+19, IK21a, JRD+23, KHS+23, LLS22, MMA+18, OCMP19, QYZ21, RHGD21, RMR21, RCS+19, SSR+18, TML+17a, TML+17b, TML+17c, WTZ+20, WMGD23, WGZ+23, ZPRD22, ZZZ21, ZNF21, CWD+21, MRSBGR+20, ZPRD23]. **verified** [TMK+16]. **Verifying** [TZG+23]. **Verilog** [IK21a, LCCS21, MKVD23, Mis22]. **version** [AS24]. **Very** [QLC20]. **Veyron** [Ano23g]. **VGG** [SCM+21]. **VGG-16** [SCM+21]. **VHDL** [PMKZ22]. **via** [dAGM23]. **Vibration** [MGZ+23]. **Virtex** [SFGB20]. **Virtex-7** [SFGB20]. **Virtex-UltraScale** [SFGB20]. **Virtual** [BWP22, FHD22, HGLD18, HGLD19, HGTD20, HGD20b, HGTD21, LCW+24, ZWL+23, HGPD20, IEE21, IEE22, KKC+16]. **Virtualization** [DK23, MTJ+22, SMP22, SVM+23, CLM+22]. **Visible** [SLB+22, ZSM20]. **Vision** [LRF+21]. **Visual** [SED+23]. **Vitamin** [AAC+23]. **Vitamin-V** [AAC+23]. **Vitruvius** [MPU+23]. **VLSI** [LLS22, YTL+23]. **vMCU** [MST+23]. **Vmin** [ZCNA16]. **Volatile** [MTT21]. **Voltage** [AMG+20, CCA+18a, CCA+18b, WCL23]. **Volume** [WA21, WAH21]. **Vortex** [ETR+20, TEYK21, TYEK21]. **VOSySmonitoRV** [CIPR21]. **VP** [APHD21b]. **VPQC** [XHY+20]. **vs** [LGB17]. **VSDFLOW** [GG18]. **VTF** [JHLD21]. **Vulnerability** [KNK+21, GYW+23]. **Vulnerable** [AHV+21, HVW+21]. **VVT** [AAC+23].

**W** [CRP+23, GZK+21, LWA+14, NRB+23, SB23]. **Wally** [HHTo23]. **WasmAndroid** [WWN23]. **wave** [KKH+20]. **Wearable** [EMMB19, HCL+21, LHC+21, PLH+22, CPL+24]. **Web** [GSDB18]. **Web-Based** [GSDB18]. **WebRISC** [MG22]. **WebRISC-V** [MG22]. **weight** [MMR+17, RSM+23]. **Western** [Ano23f]. **Wi-Fi** [WRD+17]. **Will** [Gre20]. **Win**

[Gen24]. **Winograd** [WZW+21]. **Winograd-Based** [WZW+21]. **wins** [SCR+17]. **Wireless** [ABP22, KIS20]. **Without** [MMA+18, Bis21]. **Word** [QLC20]. **Work** [HWG22, Liu21]. **Work-in-Progress** [HWG22, Liu21]. **World** [WTS21]. **Writing** [MTT21].

**x264** [WWW23]. **x86** [LF22]. **XACT** [PPS+19, PH18]. **xBGAS** [WLW+21]. **Xilinx** [KAR+19, WW19]. **XpulpNN** [GTC+20, GTC+21a, GTC+21b]. **Xuantie** [CXL+20a, CXL+20b]. **Xuantie-910** [CXL+20a, CXL+20b]. **Xvpfloat** [GFB+24].

**Years** [Pat18]. **YOLO** [QLH21, ZZW+19]. **Yun** [PCO+23].

**Zbb** [MR22]. **ZigZag** [CPLS23]. **ZUC** [WYK21]. **ZUC-256** [WYK21]. **Zynq** [dOK23].

# References

**Abella:2021:SRT**

[AAA+21] Jaume Abella, Sergi Alcaide, Jens Anders, Francisco Bas, Steffen Becker, Elke De Mulder, Nourhan Elhamawy, Frank K. Gürkaynak, Helena Handschuh, Carles Hernandez, Mike Hutter, Leonidas Kosmidis, Ilia Polian, Matthias Sauer, Stefan Wagner, and Francesco Regazzoni. Security, reliability and test aspects of the RISC-V ecosystem. In IEEE, editor, *2021 IEEE European Test Symposium (ETS)*, pages 1–10. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Anders:2023:SRD**

[AAB+23] Jens Anders, Pablo Andreu, Bernd Becker, Steffen Becker, Riccardo Cantoro, Nikolaos I. Deligiannis, Nourhan Elhamawy, Tobias Faller, Carles Hernandez, Nele Mentens, Mahnaz Namazi Rizi, Ilia Polian, Abolfazl Sajadi, Mathias Sauer, Denis Schwachhofer, Matteo Sonza Reorda, Todor Stefanov, Ilya Tuzov, Stefan Wagner, and Nuša Zidarič. A survey of recent developments in testability, safety and security of RISC-V processors. In IEEE, editor, *2023 IEEE European Test Symposium (ETS)*, pages 1–10. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Alonso:2023:VVT**

[AAC+23] Martí Alonso, David Andreu, Ramon Canal, Stefano Di Carlo, Cristiano Chenet, Juanjo Costa, Andreu Girones, Dimitris Gizopoulos, Vasileios Karakostas, Beatriz Otero, George Papadimitriou, Eva Rodríguez, and Alessandro Savino. Validation, verification, and testing (VVT) of future RISC-V powered cloud infrastructures: the Vitamin-V Horizon Europe

Project perspective. In IEEE, editor, *2023 IEEE European Test Symposium (ETS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Abella:2020:ARV**

[ABC+20] Jaume Abella, Calvin Bulla, Guillem Cabo, Francisco J. Cazorla, Adrián Cristal, Max Doblas, Roger Figueras, Alberto González, Carles Hernández, César Hernández, Víctor Jiménez, Leonidas Kosmidis, Vatistas Kostalabros, Rubén Langarita, Neiel Leyva, Guillem López-Paradís, Joan Marimon, Ricardo Martínez, Jonnatan Mendoza, Francesc Moll, Miquel Moretó, Julián Pavón, Cristóbal Ramírez, Marco A. Ramírez, Carlos Rojas, Antonio Rubio, Abraham Ruiz, Nehir Sonmez, Víctor Soria, Lluís Terés, Osman Unsal, Mateo Valero, Iván Vargas, Luís Villa, and Cristóbal Ramíiez. An academic RISC-V silicon implementation based on open-source components. In IEEE, editor, *2020 XXXV Conference on Design of Circuits and Integrated Systems (DCIS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Angioli:2023:AHA**

[ABM+23] Marco Angioli, Marcello Barbirotta, Antonio Mastrandrea, Saeid Jamili, and Mauro Olivieri. Automatic hardware accelerators reconfiguration through LinearUCB algorithms on a RISC-V processor. In IEEE, editor, *2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, pages 169–172. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Amor:2022:RVI**

[ABP22] Hela Belhadj Amor, Carolynn Bernier, and Zdeněk Přikryl. A RISC-V ISA extension for ultra-low power IoT wireless signal processing. *IEEE Transactions on Computers*, 71(4):766–778, April 2022. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**AskariHemmat:2020:RVB**

[ABW+20] MohammadHossein AskariHemmat, Olexa Bilaniuk, Sean Wagner, Yvon Savaria, and Jean-Pierre David. RISC-V barrel processor for accelerator control. In IEEE, editor, *2020 IEEE 28th Annual In-*

*ternational Symposium on Field-Programmable Custom Computing Machines (FCCM)*, page 212. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**AskariHemmat:2021:RVB**

[ABW+21] MohammadHossein AskariHemmat, Olexa Bilaniuk, Sean Wagner, Yvon Savaria, and Jean-Pierre David. RISC-V barrel processor for deep neural network acceleration. In IEEE, editor, *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**AskariHemmat:2023:QIR**

[ADF+23] MohammadHossein AskariHemmat, Théo Dupuis, Yoan Fournier, Nizar El Zarif, Matheus Cavalcante, Matteo Perotti, Frank Gürkaynak, Luca Benini, François Leduc-Primeau, Yvon Savaria, and Jean-Pierre David. Quark: an integer RISC-V vector processor for sub-byte quantized DNN inference. In IEEE, editor, *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**AlAssir:2021:ARV**

[AEAS21] Imad Al Assir, Mohamad El Iskandarani, Hadi Rayan Al Sandid, and Mazen A. R. Saghir. Arrow: a RISC-V vector accelerator for machine learning inference. *arXiv.org*, ??(??):1–6, July 15, 2021. URL `https://arxiv.org/abs/2107.07169`.

**Amarnath:2017:CNT**

[AFP+17] Aporva Amarnath, Siying Feng, Subhankar Pal, Tutu Ajayi, Austin Rovinski, and Ronald G. Dreslinski. A carbon nanotube transistor based RISC-V processor using pass transistor logic. In IEEE, editor, *2017 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017.

**Andri:2020:ERV**

[AHB20] Renzo Andri, Tomas Henriksson, and Luca Benini. Extending the RISC-V ISA for efficient RNN-based 5G radio resource management. In IEEE, editor, *2020 57th ACM/IEEE Design Automation Conference (DAC)*, pages 1–

6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Austin:2021:MIR**

[AHV+21] Todd Austin, Austin Harris, Tarunesh Verma, Shijia Wei, Alex Kisil, Misiker Aga, Valeria Bertacco, Baris Kasikci, and Mohit Tiwari. Morpheus II: a RISC-V security extension for protecting vulnerable software and hardware. In IEEE, editor, *2021 IEEE Hot Chips 33 Symposium (HCS)*, pages 1–18. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Adelt:2020:SPQ**

[AKMS20] Peer Adelt, Bastian Koppelmann, Wolfgang Mueller, and Christoph Scheytt. A scalable platform for QEMU based fault effect analysis for RISC-V hardware architectures. In IEEE, editor, *MBMV 2020 — Methods and Description Languages for Modelling and Verification of Circuits and Systems; GMM/ITG/GI-Workshop*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Adelt:2021:RIC**

[AKMS21] Peer Adelt, Bastian Koppelmann, Wolfgang Mueller, and Christoph Scheytt. Register and instruction coverage analysis for different RISC-V ISA modules. In IEEE, editor, *MBMV 2021; 24th Workshop*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Arnaud:2020:RVB**

[AMG+20] A. Arnaud, M. Miguez, J. Gak, R. Puyol, R. Garcia-Ramirez, E. Solera-Bolanos, R. Castro-Gonzalez, R. Molina-Robles, A. Chacon-Rodriguez, and R. Rimolo-Donadio. A RISC-V based medical implantable SoC for high voltage and current tissue stimulus. In IEEE, editor, *2020 IEEE 11th Latin American Symposium on Circuits & Systems (LASCAS)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Aponte-Moreno:2021:RER**

[AMRCP21] Alexander Aponte-Moreno, Felipe Restrepo-Calle, and Cesar Pedraza. Reliability evaluation of RISC-V and ARM microprocessors through a new fault injection tool. In IEEE,

editor, *2021 IEEE 22nd Latin American Test Symposium (LATS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Andersson:2020:DNV**

[And20] Jan Andersson. Development of a NOEL-V RISC-V SoC targeting space applications. In IEEE, editor, *2020 50th Annual IEEE/IFIP International Conference on Dependable Systems and Networks Workshops (DSN-W)*, pages 66–67. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Anonymous:2020:RVE**

[Ano20] Anonymous. RISC-V embedded variant RV32E now fully supported by SEGGER's floating-point library. Web site, September 21, 2020. URL `https://www.design-reuse.com/news/48672/segger-s-floating-point-library-risc-v-rv32e.html`.

**Anonymous:2021:SFS**

[Ano21] Anonymous. Source files for SiFive's Freedom platforms. Web document., 2021. URL `https://github.com/sifive/freedom`.

**Anonymous:2022:TRV**

[Ano22] Anonymous. Tutorial #1: RISC-V computer system designed for cyber-security. In IEEE, editor, *2022 International Conference on IC Design and Technology (ICICDT)*, page xxxi. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Anonymous:2023:BBO**

[Ano23a] Anonymous. BOOM: The Berkeley out-of-order RISC-V processor. Web site., 2023. URL `https://github.com/riscv-boom`.

**Anonymous:2023:CRV**

[Ano23b] Anonymous. China RISC-V Alliance. Chinese-language Web site, 2023. URL `http://crva.ict.ac.cn/`.

**Anonymous:2023:OSH**

[Ano23c] Anonymous. Open-source high-performance RISC-V processor. Web site., 2023. URL `https://github.com/OpenXiangShan/XiangShan`.

**Anonymous:2023:PHP**

[Ano23d] Anonymous. P870 high-performance RISC-V processor. In IEEE, editor, *2023 IEEE Hot Chips 35 Symposium (HCS)*, pages 1–19. IEEE Computer Society Press, 1109 Spring Street,

Suite 300, Silver Spring, MD 20910, USA, 2023.

**Anonymous:2023:RCG**

[Ano23e] Anonymous. Rocket Chip generator, 2023. URL `https://github.com/chipsalliance/rocket-chip`.

**Anonymous:2023:SRV**

[Ano23f] Anonymous. SweRV RISC-V core 1.1 from Western Digital. Web site., 2023. URL `https://github.com/chipsalliance/Cores-VeeR-EH1`; `https://github.com/westerndigitalcorporation/swerv_eh1`.

**Anonymous:2023:VVD**

[Ano23g] Anonymous. Veyron V1 data center-class RISC-V processor. In IEEE, editor, *2023 IEEE Hot Chips 35 Symposium (HCS)*, pages 1–16. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Antonov:2022:SOR**

[Ant22] Alexander Antonov. Superscalar out-of-order RISC-V ASIP based on programmable hardware generator with decoupled computations and flow control. In IEEE, editor, *2022 11th Mediterranean Conference on Embedded Computing (MECO)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Asanovic:2014:ISS**

[AP14] K. Asanović and D. A. Patterson. Instruction sets should be free: the case for RISC-V. Technical Report UCB/EECS-2014-146, Department of Electrical Engineering and Computer Science, University of California, Berkeley, Berkeley, CA, USA, August 6, 2014. 7 pp. URL `https://www2.eecs.berkeley.edu/Pubs/TechRpts/2014/EECS-2014-146.pdf`.

**Ahmadi-Pour:2021:CRV**

[APHD21a] Sallar Ahmadi-Pour, Vladimir Herdt, and Rolf Drechsler. Constrained random verification for RISC-V: Overview, evaluation and discussion. In IEEE, editor, *MBMV 2021; 24th Workshop*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Ahmadi-Pour:2021:RVA**

[APHD21b] Sallar Ahmadi-Pour, Vladimir Herdt, and Rolf Drechsler. RISC-V AMS VP: an open source evaluation platform for cyber-physical systems. In IEEE, editor, *2021 Forum on specification & Design Languages (FDL)*, pages 01–07. IEEE Com-

puter Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Ahmadi-Pour:2022:MFA**

[APHD22] Sallar Ahmadi-Pour, Vladimir Herdt, and Rolf Drechsler. The MicroRV32 framework: An accessible and configurable open source RISC-V cross-level platform for education and research. *Journal of Systems Architecture*, 133:102757, 2022. CODEN JSARFB. ISSN 1383-7621 (print), 1873-6165 (electronic). URL `https://www.sciencedirect.com/science/article/pii/S1383762122002429`.

**Ahmadi-Pour:2022:TMS**

[APSH+22] Sallar Ahmadi-Pour, Sangeet Saha, Vladimir Herdt, Rolf Drechsler, and Klaus McDonald-Maier. Task mapping and scheduling in FPGA-based heterogeneous real-time systems: a RISC-V case-study. In IEEE, editor, *2022 25th Euromicro Conference on Digital System Design (DSD)*, pages 134–141. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Annink:2022:PSE**

[ARH+22] Edian B. Annink, Gerard Rauwerda, Edwin Hakkennes, Alessandra Menicucci, Stefano Di Mascio, Gianluca Furano, and Marco Ottavi. Preventing soft errors and hardware trojans in RISC-V cores. In IEEE, editor, *2022 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Alizadeh:2018:ERV**

[AS18] M. Alizadeh and M. Sharifkhani. Extending RISC-V ISA for accelerating the H.265/HEVC deblocking filter. In IEEE, editor, *2018 8th International Conference on Computer and Knowledge Engineering (ICCKE)*, pages 126–129. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Adit:2022:PLT**

[AS22] Neil Adit and Adrian Sampson. Performance left on the table: an evaluation of compiler autovectorization for RISC-V. *IEEE Micro*, 42(5):41–48, September/October 2022. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

**Asano:2024:SBE**

[AS24] Tamon Asano and Takeshi Sugawara. Simulation-based evaluation of bit-interaction side-channel leakage on RISC-V: extended version. *Journal of Cryptographic Engineering*, 14(1):165–180, April 2024. CODEN ???? ISSN 2190-8508 (print), 2190-8516 (electronic). URL `https://link.springer.com/article/10.1007/s13389-023-00319-z`.

**Adel:2021:IFV**

[ASE+21] Abdelrahman Adel, Dina Saad, Mahmoud Abd El Mawgoed, Mohamed Sharshar, Zyad Ahmed, Hala Ibrahim, and Hassan Mostafa. Implementation and functional verification of RISC-V core for secure IoT applications. In IEEE, editor, *2021 International Conference on Microelectronics (ICM)*, pages 254–257. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Auer:2019:SAR**

[ASH19] Lukas Auer, Christian Skubich, and Matthias Hiller. A security architecture for RISC-V based IoT devices. In IEEE, editor, *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1154–1159. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Ali:2021:VPU**

[AvAG21] Muhammad Ali, Matthias von Ameln, and Diana Goehringer. Vector processing unit: a RISC-V based SIMD co-processor for embedded processing. In IEEE, editor, *2021 24th Euromicro Conference on Digital System Design (DSD)*, pages 30–34. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Alder:2022:FPU**

[AVS+22] Fritz Alder, Jo Van Bulck, Jesse Spielman, David Oswald, and Frank Piessens. Faulty point unit: ABI poisoning attacks on trusted execution environments. *Digital Threats: Research and Practice (DTRAP)*, 3 (2):13:1–13:26, June 2022. CODEN ???? ISSN 2692-1626 (print), 2576-5337 (electronic). URL `https://dl.acm.org/doi/10.1145/3491264`.

**AskariHemmat:2023:BAP**

[AWB+23] MohammadHossein AskariHemmat, Sean Wagner, Olexa Bilaniuk, Yassine Hariri, Yvon Savaria, and Jean-Pierre David. BARVINN:

Arbitrary precision DNN accelerator controlled by a RISC-V CPU. In IEEE, editor, *2023 28th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages 483–489. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Azad:2023:RRV**

[AYA+23] Zahra Azad, Guowei Yang, Rashmi Agrawal, Daniel Petrisko, Michael Taylor, and Ajay Joshi. RISE: RISC-V SoC for En/Decryption acceleration on the edge for homomorphic encryption. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 31(10):1523–1536, 2023. CODEN IEVSE9. ISSN 1063-8210 (print), 1557-9999 (electronic).

**Barriga:2020:RVP**

[Bar20] Angel Barriga. RISC-V processors design: a methodology for cores development. In IEEE, editor, *2020 XXXV Conference on Design of Circuits and Integrated Systems (DCIS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Baumann:2017:HNS**

[Bau17] Andrew Baumann. Hardware is the new software. In ACM, editor, *HotOS '17: Workshop on Hot Topics in Operating Systems, Whistler, BC, Canada, May 7–10, 2017*, pages 132–137. ACM Press, New York, NY 10036, USA, 2017. URL `https://dl.acm.org/doi/pdf/10.1145/3102980.3103002`.

**Balas:2021:RVR**

[BB21] Robert Balas and Luca Benini. RISC-V for real-time MCUs — software optimization and microarchitectural gap analysis. In IEEE, editor, *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 874–877. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Burgess:2017:ISC**

[BBdD17] Neil Burgess, Javier Bruguera, and Florent de Dinechin, editors. *2017 IEEE 24th Symposium on Computer Arithmetic (ARITH 24), London, UK, 24–26 July 2017*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017. ISBN 1-5386-1966-0 (print), 1-5386-1965-2, 1-5386-1964-4. ISSN 1063-6889. LCCN QA76.9.C62 S95 2017. URL `http:`

//ieeexplore.ieee.org/servlet/opac?punumber=8019911.

**B:2023:HPS**

[BBV+23] Anil Kumar D B, Bansilal Bairwa, Bhadriraju Vamsidath, Ujwal V, Tharun P, and Tushaar Rao. HDL programming and sequential circuitry for multicore RISC-V processor. In IEEE, editor, *2023 International Conference on Smart Systems for applications in Electrical Sciences (ICSSES)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Birari:2020:RVI**

[BBVB20] Akshay Birari, Piyush Birla, Kuruvilla Varghese, and Amrutur Bharadwaj. A RISC-V ISA compatible processor IP. In IEEE, editor, *2020 24th International Symposium on VLSI Design and Test (VDAT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Bellocchi:2021:RVB**

[BCCM21] Gianluca Bellocchi, Alessandro Capotondi, Francesco Conti, and Andrea Marongiu. A RISC-V-based FPGA overlay to simplify embedded accelerator deployment. In IEEE, editor, *2021 24th Euromicro Conference on Digital System Design (DSD)*, pages 9–17. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Barbirotta:2021:FTS**

[BCM+21] Marcello Barbirotta, Abdallah Cheikh, Antonio Mastrandrea, Francesco Menichelli, Francesco Vigli, and Mauro Olivieri. A fault tolerant soft-core obtained from an interleaved-multithreading RISC-V microprocessor design. In IEEE, editor, *2021 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Boubakri:2021:OPT**

[BCZ21a] Marouene Boubakri, Fausto Chiatante, and Belhassen Zouari. Open portable trusted execution environment framework for RISC-V. In IEEE, editor, *2021 IEEE 19th International Conference on Embedded and Ubiquitous Computing (EUC)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Boubakri:2021:TFT**

[BCZ21b] Marouene Boubakri, Fausto Chiatante, and Belhassen Zouari. Towards a firmware TPM on RISC-V. In IEEE, editor, *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 647–650. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Bocco:2019:DPN**

[BDdD19a] Andrea Bocco, Yves Durand, and Florent de Dinechin. Dynamic precision numerics using a variable-precision UNUM Type I HW coprocessor. In Takagi et al. [TBL19], pages 104–107. ISBN 1-72813-366-1. ISSN 1063-6889.

**Bocco:2019:SSM**

[BDdD19b] Andrea Bocco, Yves Durand, and Florent de Dinechin. SMURF: Scalar Multiple-precision Unum RISC-V Floating-point accelerator for scientific computing. In Gustafson and Dimitrov [GD19], pages 1:1–1:8. ISBN 1-4503-7139-6. LCCN ???? URL `https://hal.inria.fr/hal-02087098`.

**Benini:2023:NDC**

[Ben23] Luca Benini. From nanodrones to cars — a RISC-V open platform for next-generation vehicles. In IEEE, editor, *2023 9th International Workshop on Advances in Sensors and Interfaces (IWASI)*, page 8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Bove:2023:BSS**

[BF23] Davide Bove and Julian Funk. Basic secure services for standard RISC-V architectures. *Computers & Security*, 133(??):??, October 2023. CODEN CPSEDU. ISSN 0167-4048 (print), 1872-6208 (electronic). URL `http://www.sciencedirect.com/science/article/pii/S0167404823003255`.

**Bohmer:2023:NRT**

[BFC+23] Kevin Böhmer, Bruno Forlin, Carlo Cazzaniga, Paolo Rech, Gianluca Furano, Nikolaos Alachiotis, and Marco Ottavi. Neutron radiation tests of the NEORV32 RISC-V SoC on flash-based FPGAs. In IEEE, editor, *2023 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Bartolini:2022:MCP**

[BFP+22] Andrea Bartolini, Federico Ficarelli, Emanuele Parisi, Francesco Beneventi, Francesco Barchi, Daniele Gregori, Fabrizio Magugliani, Marco Cicala, Cosimo Gianfreda, Daniele Cesarini, Andrea Acquaviva, and Luca Benini. Monte Cimone: Paving the road for the first generation of RISC-V high-performance computers. In IEEE, editor, *2022 IEEE 35th International System-on-Chip Conference (SOCC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Budi:2018:RVI**

[BGVB18] Suseela Budi, Pradeep Gupta, Kuruvilla Varghese, and Amrutur Bharadwaj. A RISC-V ISA compatible processor IP for SoC. In IEEE, editor, *2018 International Symposium on Devices, Circuits and Systems (ISDCS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Bruns:2023:PVU**

[BHD23] Niklas Bruns, Vladimir Herdt, and Rolf Drechsler. Processor verification using symbolic execution: a RISC-V case-study. In IEEE, editor, *2023 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Bruns:2021:TRV**

[BHGD21] Niklas Bruns, Vladimir Herdt, Daniel Große, and Rolf Drechsler. Toward RISC-V CSR compliance testing. *IEEE Embedded Systems Letters*, 13(4):202–205, 2021. ISSN 1943-0663 (print), 1943-0671 (electronic).

**Bailey:2018:GMS**

[BHR+18] Stevo Bailey, Jaeduk Han, Paul Rigge, Richard Lin, Eric Chang, Howard Mao, Zhongkai Wang, Chick Markley, Adam Izraelevitz, Angie Wang, Nathan Narevsky, Woorham Bae, Steve Shauck, Sergio Montano, Justin Norsworthy, Munir Razzaque, Wen Hau Ma, Akalu Lentiro, Matthew Doerflein, Darin Heckendorn, Jim McGrath, Franco DeSeta, Ronen Shoham, Mike Stellfox, Mark Snowden, Joseph Cole, Dan Fuhrman, Brian Richards, Jonathan Bachrach, Elad Alon, and Borivoje Nikolić. A generated multirate signal analysis

RISC-V SoC in 16nm FinFET. In IEEE, editor, *2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pages 285–288. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Bruschi:2021:GHC**

[BHT+21] Nazareno Bruschi, Germain Haugou, Giuseppe Tagliavini, Francesco Conti, Luca Benini, and Davide Rossi. GVSoC: a highly configurable, fast and accurate full-platform simulator for RISC-V based IoT processors. In IEEE, editor, *2021 IEEE 39th International Conference on Computer Design (ICCD)*, pages 409–416. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Biswas:2021:CSI**

[Bis21] Arnab Kumar Biswas. Cryptographic software IP protection without compromising performance or timing side-channel leakage. *ACM Transactions on Architecture and Code Optimization*, 18(2):20:1–20:20, March 2021. CODEN ???? ISSN 1544-3566 (print), 1544-3973 (electronic). URL `https://dl.acm.org/doi/10.1145/3443707`.

**Barral:2023:ESR**

[BJN23] Hadrien Barral, Georges-Axel Jaloyan, and David Naccache. Emoji shellcoding in RISC-V. In IEEE, editor, *2023* IEEE Security and Privacy *Workshops (SPW)*, pages 255–263. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Bavier:2023:VNF**

[BKdLSGL23] Eric Bavier, Nicholas Knight, Hugues de Lassus Saint-Geniès, and Eric Love. Vectorized nonlinear functions with the RISC-V vector extension. In IEEE [IEE23], pages 127–130. LCCN ????

**B:2022:MMT**

[BKS22] Karunatharaka B, Sakshi Kamal, and Sharvani G S. Minimal multi-tasking operating system for RISC-V. In IEEE, editor, *2022 4th International Conference on Advances in Computing, Communication Control and Networking (ICAC3N)*, pages 2267–2270. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Barbirotta:2020:FRA**

[BMM+20] Marcello Barbirotta, Antonio Mastrandrea, Francesco Menichelli, Francesco Vigli, Luigi Blasi, Abdallah Cheikh, Stefano Sordillo, Fabio Di Gennaro, and Mauro Olivieri. Fault resilience analysis of a RISC-V microprocessor design through a dedicated UVM environment. In IEEE, editor, *2020 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Borin:2023:IAP**

[Bor23] Edson Borin. *An Introduction to Assembly Programming with RISC-V*. ????, ????, 2023. ISBN 65-00-15811-3. 189 pp. LCCN ????

**Bora:2021:HPC**

[BP21] Satyajit Bora and Roy Paily. A high-performance core micro-architecture based on RISC-V ISA for low power applications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 68(6):2132–2136, 2021. ISSN 1549-7747 (print), 1558-3791 (electronic).

**Bertaccini:2022:MNE**

[BPF+22] Luca Bertaccini, Gianna Paulin, Tim Fischer, Stefan Mach, and Luca Benini. MiniFloat-NN and ExSdotp: an ISA extension and a modular open hardware unit for low-precision training on RISC-V cores. In IEEE [IEE22], pages 1–8. ISBN 1-66547-827-6, 1-66547-828-4. LCCN ????

**Bertaccini:2021:TFL**

[BPM+21] Luca Bertaccini, Matteo Perotti, Stefan Mach, Pasquale Davide Schiavone, Florian Zaruba, and Luca Benini. Tiny-FPU: Low-cost floating-point support for small RISC-V MCU cores. In IEEE, editor, *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Borowski:2023:ABT**

[BPS+23] Michal Borowski, Chandrajit Pal, Sangeet Saha, Ludovico Poli, Xiaojun Zhai, and Klaus D. McDonald-Maier. Anomaly behaviour tracing of CHERI-RISC V using hardware–software co-design. In IEEE, editor, *2023 21st IEEE Interregional NEWCAS Conference (NEWCAS)*, pages 1–5. IEEE Computer Society

Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Brohet:2024:STM**

[BR24] Marco Brohet and Francesco Regazzoni. A survey on thwarting memory corruption in RISC-V. *ACM Computing Surveys*, 56(2): 28:1–28:??, February 2024. CODEN CMSVAN. ISSN 0360-0300 (print), 1557-7341 (electronic). URL `https://dl.acm.org/doi/10.1145/3604906`.

**Bailey:2019:MSR**

[BRH+19] Steven Bailey, Paul Rigge, Jaeduk Han, Richard Lin, Eric Y. Chang, Howard Mao, Zhongkai Wang, Chick Markley, Adam M. Izraelevitz, Angie Wang, Nathan Narevsky, Woorham Bae, Steve Shauck, Sergio Montano, Justin Norsworthy, Munir Razzaque, Wen Hau Ma, Akalu Lentiro, Matthew Doerflein, Darin Heckendorn, Jim McGrath, Franco DeSeta, Ronen Shoham, Mike Stellfox, Mark Snowden, Joseph Cole, Daniel R. Fuhrman, Brian Richards, Jonathan Bachrach, Elad Alon, and Borivoje Nikolić. A mixed-signal RISC-V signal analysis SoC generator with a 16-nm FinFET instance. *IEEE Journal of Solid-State Circuits*, 54(10):2786–2801, 2019. CODEN IJSCBC. ISSN 0018-9200 (print), 1558-173X (electronic).

**Babu:2021:EBM**

[BSSW21] P. S. Babu, Snehashri Sivaraman, Deepa N. Sarma, and Tripti S. Warrier. Evaluation of bit manipulation instructions in optimization of size and speed in RISC-V. In IEEE, editor, *2021 34th International Conference on VLSI Design and 2021 20th International Conference on Embedded Systems (VLSID)*, pages 54–59. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Bai:2021:BER**

[BSZ+21] Chen Bai, Qi Sun, Jianwang Zhai, Yuzhe Ma, Bei Yu, and Martin D. F. Wong. BOOM-Explorer: RISC-V BOOM microarchitecture design space exploration framework. In IEEE, editor, *2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, pages 1–9. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Bai:2024:BER**

[BSZ+24] Chen Bai, Qi Sun, Jianwang Zhai, Yuzhe Ma, Bei Yu, and Martin D. F. Wong.

BOOM-Explorer: RISC-V BOOM microarchitecture design space exploration. *ACM Transactions on Design Automation of Electronic Systems*, 29(1): 20:1–20:??, January 2024. CODEN ATASFO. ISSN 1084-4309 (print), 1557-7309 (electronic). URL `https://dl.acm.org/doi/10.1145/3630013`.

**Boseler:2022:CVP**

[BWP22] Felix Böseler, Jörg Walter, and Behnam Razi Perjikolaei. A comparison of virtual platform simulation solutions for timing prediction of small RISC-V based SoCs. In IEEE, editor, *2022 Forum on Specification & Design Languages (FDL)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Bai:2021:HFI**

[BWZ+21] Jiyuan Bai, Xiang Wang, Zikang Zhang, Chang Cai, and Gengsheng Chen. A hierarchical fault injection system for RISC-V processors targeting single event upsets in flip-flops. In IEEE, editor, *2021 IEEE 14th International Conference on ASIC (ASICON)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Bertuletti:2023:EPP**

[BZVCB23] Marco Bertuletti, Yichao Zhang, Alessandro Vanelli-Coralli, and Luca Benini. Efficient parallelization of 5G-PUSCH on a scalable RISC-V many-core processor. In IEEE, editor, *2023 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Chuah:2023:FVS**

[CAL23] Czea Sie Chuah, Christian Appold, and Tim Leinmueller. Formal verification of security properties on RISC-V processors. In IEEE, editor, *2023 21st ACM-IEEE International Symposium on Formal Methods and Models for System Design (MEMOCODE)*, pages 159–168. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Chiu:2018:CRT**

[CCA+18a] Pi-Feng Chiu, Christopher Celio, Krste Asanović, Borivoje Nikolić, and David Patterson. Cache resiliency techniques for a low-voltage RISC-V out-of-order processor in 28-nm CMOS. *IEEE Solid-State*

*Circuits Letters*, 1(12):229–232, 2018. ISSN 2573-9603.

**Chiu:2018:ORV**

[CCA+18b] Pi-Feng Chiu, Christopher Celio, Krste Asanović, David Patterson, and Borivoje Nikolić. An out-of-order RISC-V processor with resilient low-voltage operation in 28NM CMOS. In IEEE, editor, *2018 IEEE Symposium on VLSI Circuits*, pages 61–62. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Calicchia:2019:DSP**

[CCC+19] L. Calicchia, V. Ciotoli, G. C. Cardarilli, L. di Nunzio, R. Fazzolari, A. Nannarelli, and M. Re. Digital signal processing accelerator for RISC-V. In IEEE, editor, *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pages 703–706. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Cabo:2022:DRV**

[CCC+22] Guillem Cabo, Gerard Candón, Xavier Carril, Max Doblas, Marc Domínguez, Alberto González, César Hernández, Víctor Jiménez, Vatistas Kostalampros, Rubén Langarita, Neiél Leyva, Guillem López-Paradís, Jonnatan Mendoza, Francesco Minervini, Julián Pavón, Cristóbal Ramírez, Narcís Rodas, Enrico Reggiani, Mario Rodríguez, Carlos Rojas, Abraham Ruiz, Víctor Soria, Alejandro Suanes, Iván Vargas, Roger Figueras, Pau Fontova, Joan Marimon, Víctor Montabes, Adrián Cristal, Carles Hernández, Ricardo Martínez, Miquel Moretó, Francesc Moll, Oscar Palomar, Marco A. Ramírez, Antonio Rubio, Jordi Sacristán, Francesc Serra-Graells, Nehir Sonmez, Lluís Terés, Osman Unsal, Mateo Valero, and Luís Villa. DVINO: a RISC-V vector processor implemented in 65nm technology. In IEEE, editor, *2022 37th Conference on Design of Circuits and Integrated Circuits (DCIS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Cappellone:2020:BST**

[CDF+20] Danilo Cappellone, Stefano Di Mascio, Gianluca Furano, Alessandra Menicucci, and Marco Ottavi. On-board satellite telemetry forecasting with RNN on RISC-V based multicore processor. In IEEE, ed-

itor, *2020 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Cassano:2022:RVR**

[CDP+22] Luca Cassano, Stefano Di Mascio, Alessandro Palumbo, Alessandra Menicucci, Gianluca Furano, Giuseppe Bianchi, and Marco Ottavi. Is RISC-V ready for space? A security perspective. In IEEE, editor, *2022 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Cloosters:2024:MCB**

[CDW+24] Tobias Cloosters, Oussama Draissi, Johannes Willbold, Thorsten Holz, and Lucas Davi. Memory corruption at the border of trusted execution. *IEEE Security & Privacy*, 22(4):87–96, July/August 2024. ISSN 1540-7993 (print), 1558-4046 (electronic).

**Cannizzaro:2023:ERV**

[CG23] Michael J. Cannizzaro and Alan D. George. Evaluation of RISC-V silicon under neutron radiation. In IEEE, editor, *2023 IEEE Aerospace Conference*, pages 1–9. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Cannizzaro:2021:RVB**

[CGG21] Michael J. Cannizzaro, Evan W. Gretok, and Alan D. George. RISC-V benchmarking for onboard sensor processing. In IEEE, editor, *2021 IEEE Space Computing Conference (SCC)*, pages 46–59. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Chisnall:2023:HDI**

[Chi23] David Chisnall. How to design an ISA: The popularity of RISC-V has led many to try designing instruction sets. *ACM Queue: Tomorrow's Computing Today*, 21 (6):27–46, November 2023. CODEN AQCUAE. ISSN 1542-7730 (print), 1542-7749 (electronic). URL `https://dl.acm.org/doi/10.1145/3639445`.

**Chisnall:2024:HDI**

[Chi24] David Chisnall. How to design an ISA. *Communications of the Associa-*

*tion for Computing Machinery*, 67(5):60–66, May 2024. CODEN CACMA2. ISSN 0001-0782 (print), 1557-7317 (electronic). URL `https://dl.acm.org/doi/10.1145/3640538`.

**Cho:2018:IMD**

[Cho18] Hyungmin Cho. Impact of microarchitectural differences of RISC-V processor cores on soft error effects. *IEEE Access*, 6: 41302–41313, 2018. ISSN 2169-3536. See correction [Cho19].

**Cho:2019:CIM**

[Cho19] Hyungmin Cho. Correction to "Impact of Microarchitectural Differences of RISC-V Processor Cores on Soft Error Effects". *IEEE Access*, 7:35034, 2019. ISSN 2169-3536. See [Cho18].

**Cilardo:2021:MES**

[Cil21] Alessandro Cilardo. Memory encryption support for an FPGA-based RISC-V implementation. In IEEE, editor, *2021 16th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Caforio:2021:VMC**

[CIPR21] Flavia Caforio, Pierpaolo Iannicelli, Michele Paolino, and Daniel Raho. VOSyS-monitoRV: a mixed-criticality solution on Linux-capable RISC-V platforms. In IEEE, editor, *2021 10th Mediterranean Conference on Embedded Computing (MECO)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Chupilko:2018:TPG**

[CKK+18] Mikhail Chupilko, Alexander Kamkin, Artem Kotsynyak, Alexander Protsenko, Sergey Smolov, and Andrei Tatarnikov. Test program generator MicroTESK for RISC-V. In IEEE, editor, *2018 19th International Workshop on Microprocessor and SOC Test and Verification (MTV)*, pages 6–11. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Chupilko:2019:OSV**

[CKP19] Mikhail Chupilko, Alexander Kamkin, and Alexander Protsenko. Open-source validation suite for RISC-V. In IEEE, editor, *2019 20th International Workshop on Microprocessor/*

*SoC Test, Security and Verification (MTV)*, pages 7–12. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Charaf:2021:RCE**

[CKTG21] Najdet Charaf, Ahmed Kamaleldin, Martin Thümmler, and Diana Göhringer. RV-CAP: Enabling dynamic partial reconfiguration for FPGA-Based RISC-V System-on-Chip. In IEEE, editor, *2021 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*, pages 172–179. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Chen:2022:CRV**

[CKTK22] Gregory K. Chen, Phil C. Knag, Carlos Tokunaga, and Ram K. Krishnamurthy. An 8-core RISC-V processor with compute near last level cache in Intel 4 CMOS. In IEEE, editor, *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, pages 68–69. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Chen:2023:ECR**

[CKTK23] Gregory K. Chen, Phil C. Knag, Carlos Tokunaga, and Ram K. Krishnamurthy. An eight-core RISC-V processor with compute near last level cache in Intel 4 CMOS. *IEEE Journal of Solid-State Circuits*, 58(4):1117–1128, 2023. CODEN IJSCBC. ISSN 0018-9200 (print), 1558-173X (electronic).

**Chen:2020:EOT**

[CLC+20] Yi-Ru Chen, Hui-Hsin Liao, Chia-Hsuan Chang, Che-Chia Lin, Chao-Lin Lee, Yuan-Ming Chang, Chun-Chieh Yang, and Jenq-Kuen Lee. Experiments and optimizations for TVM on RISC-V architectures with P extension. In IEEE, editor, *2020 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Chen:2022:DUL**

[CLM+22] Jiahao Chen, Dingji Li, Zeyu Mi, Yuxuan Liu, Binyu Zang, Haibing Guan, and Haibo Chen. DuVisor: A user-level hypervisor through delegated virtualization,. *arXiv.org*, ?? (??):1–17, January 22, 2022.

URL `https://arxiv.org/abs/2201.09652`.

**Ciocirlan:2021:AEPb**

[CLR+21a] Stefan Dan Ciocirlan, Dumitrel Loghin, Lavanya Ramapantulu, Nicolae pu , and Yong Meng Teo. The accuracy and efficiency of posit arithmetic. In IEEE, editor, *2021 IEEE 39th International Conference on Computer Design (ICCD)*, pages 83–87. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Ciocirlan:2021:AEPa**

[CLR+21b] Stefan Dan Ciocirlan, Dumitrel Loghin, Lavanya Ramapantulu, Nicolae Tapus, and Yong Meng Teo. The accuracy and efficiency of posit arithmetic. *arXiv.org*, ??(??), September 16, 2021.

**Cui:2023:RVI**

[CLW23] Enfang Cui, Tianzheng Li, and Qian Wei. RISC-V instruction set architecture extensions: a survey. *IEEE Access*, 11: 24696–24711, 2023. ISSN 2169-3536.

**Chen:2021:SEE**

[CLWL21] Quanxiu Chen, Yi Liu, Zhenyu Wu, and Jian Liao. A single event effect simulation method for RISC-V processor. In IEEE, editor, *2021 IEEE 15th International Conference on Anti-counterfeiting, Security, and Identification (ASID)*, pages 106–110. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Castro:2021:EDP**

[CMV21] Jairo Walber Abdala Castro and Aurelio Morales-Villanueva. Exploring dynamic partial reconfiguration in a tightly-coupled coprocessor attached to a RISC-V soft-processor on a FPGA. In IEEE, editor, *2021 IEEE XXVIII International Conference on Electronics, Electrical Engineering and Computing (INTERCON)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Cieslak:2019:RMI**

[COMP19] Sebastian Cieslak, Adrian Oleksiak, Krzysztof Marcinek, and Witold A. Pleskacz. Retargeting the MIPS-II CPU core to the RISC-V architecture. In IEEE, editor, *2019 MIXDES — 26th International Conference "Mixed Design of Integrated Circuits and Systems"*, pages 261–264. IEEE Computer Society Press, 1109 Spring Street, Suite

300, Silver Spring, MD 20910, USA, 2019.

**Conti:2023:MHR**

[CPG+23] Francesco Conti, Gianna Paulin, Angelo Garofalo, Davide Rossi, Alfio Di Mauro, Georg Rutishauser, Gianmarco Ottavi, Manuel Eggimann, Hayate Okuhara, and Luca Benini. Marsellus: a heterogeneous RISC-V AI-IoT end-node SoC with 2–8 b DNN acceleration and 30%-boost adaptive body biasing. *IEEE Journal of Solid-State Circuits*, pages 1–15, 2023. CODEN IJSCBC. ISSN 0018-9200 (print), 1558-173X (electronic).

**Choi:2024:DNA**

[CPL+24] Eunjin Choi, Jina Park, Kyeongwon Lee, Jae-Jin Lee, Kyuseung Han, and Woojoo Lee. Day Night architecture: Development of an ultra-low power RISC-V processor for wearable anomaly detection. *Journal of Systems Architecture*, 152:103161, 2024. CODEN JSARFB. ISSN 1383-7621 (print), 1873-6165 (electronic). URL `https://www.sciencedirect.com/science/article/pii/S1383762124000985`.

**Chen:2023:PMZ**

[CPLS23] Yulong Chen, YanJie Pei, Xiang Lu, and Mengyao Shi. Point multiplication ZigZag: an optimized coprocessor architecture design for SM2/3 based on RISC-V. In IEEE, editor, *ICC 2023 — IEEE International Conference on Communications*, pages 3793–3798. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Chatzopoulos:2023:EEO**

[CPWG23] Odysseas Chatzopoulos, George Papadimitriou, Wing Shek Wong, and Dimitris Gizopoulos. Energy efficiency of out-of-order CPUs: Comparative study and microarchitectural hotspot characterization of RISC-V designs. In IEEE, editor, *2023 IEEE International Symposium on Workload Characterization (IISWC)*, pages 216–220. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Castells-Rufas:2023:EEP**

[CRMR+23] David Castells-Rufas, Xavier Martorell, Aleix Roca, Alexander Kropotov, Xavier Teruel, Teresa Cervero, and John D. Davis. Ethernet emulation over PCIe for RISC-V software development vehicles. In IEEE, editor, *2023 38th Conference on Design of Circuits and Integrated Systems (DCIS)*,

pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Conti:2023:WAI**

[CRP+23] Francesco Conti, Davide Rossi, Gianna Paulin, Angelo Garofalo, Alfio Di Mauro, Georg Rutishauser, Gianmarco Ottavi, Manuel Eggimann, Hayate Okuhara, Vincent Huard, Olivier Montfort, Lionel Jure, Nils Exibard, Pascal Gouedo, Mathieu Louvat, Emmanuel Botte, and Luca Benini. 22.1 A 12.4TOPS/W @ 136GOPS AI-IoT System-on-Chip with 16 RISC-V, 2-to-8b precision-scalable DNN acceleration and 30%-boost adaptive body biasing. In IEEE, editor, *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, pages 21–23. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Cococcioni:2021:VPO**

[CRRS21] Marco Cococcioni, Federico Rossi, Emanuele Ruffaldi, and Sergio Saponara. Vectorizing posit operations on RISC-V for faster deep neural networks: experiments and comparison with ARM SVE. *Neural Computing and Applications*, 33 (16):10575–10585, February 2021. ISSN 1433-3058.

**Cococcioni:2022:LPP**

[CRRS22] Marco Cococcioni, Federico Rossi, Emanuele Ruffaldi, and Sergio Saponara. A lightweight posit processing unit for RISC-V processors in deep neural network applications. *IEEE Transactions on Emerging Topics in Computing*, 10(4):1898–1908, October/December 2022. ISSN 2168-6750 (print), 2376-4562 (electronic).

**Cheikh:2021:KDV**

[CSM+21] A. Cheikh, S. Sordillo, A. Mastrandrea, F. Menichelli, G. Scotti, and M. Olivieri. Klessydra-T: Designing vector coprocessors for multithreaded edge-computing cores. *IEEE Micro*, 41(2): 64–71, March/April 2021. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

**Choudhury:2022:ORV**

[CSM22] Ananya Choudhury, Saroja V. Siddamal, and Jayashree Mallidue. An optimized RISC-V processor with five stage pipelining using Tournament Branch Predictor for efficient performance. In IEEE, editor, *2022 International Conference on Distributed Computing, VLSI, Electrical Circuits*

*and Robotics (DISCOVER)*, pages 57–60. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Cuomo:2023:TRV**

[CSO+23] Luca Cuomo, Claudio Scordino, Alessandro Ottaviano, Nils Wistoff, Robert Balas, Luca Benini, Errico Guidieri, and Ida Maria Savino. Towards a RISC-V open platform for next-generation automotive ECUs. In IEEE, editor, *2023 12th Mediterranean Conference on Embedded Computing (MECO)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Cavalcante:2020:AGS**

[CSZ+20] Matheus Cavalcante, Fabian Schuiki, Florian Zaruba, Michael Schaffner, and Luca Benini. Ara: a 1-GHz+ scalable and energy-efficient RISC-V vector processor with multiprecision floating-point support in 22-nm FD-SOI. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 28 (2):530–543, 2020. CODEN IEVSE9. ISSN 1063-8210 (print), 1557-9999 (electronic).

**Cai:2018:IDR**

[CTN18] Jingyong Cai, Masashi Takemoto, and Hironori Nakajo. Implementation of DNN on a RISC-V open source microprocessor for IoT devices. In IEEE, editor, *2018 IEEE 7th Global Conference on Consumer Electronics (GCCE)*, pages 295–299. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Cosimi:2022:AHS**

[CTSG22] Francesco Cosimi, Fabrizio Tronci, Sergio Saponara, and Paolo Gai. Analysis, hardware specification and design of a programmable performance monitoring unit (PPMU) for RISC-V ECUs. In IEEE, editor, *2022 IEEE International Conference on Smart Computing (SMARTCOMP)*, pages 213–218. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Chander:2022:SRV**

[CV22] V. Naveen Chander and Kuruvilla Varghese. A soft RISC-V vector processor for Edge-AI. In IEEE, editor, *2022 35th International Conference on VLSI Design and 2022 21st International Conference on Em-*

*bedded Systems (VLSID)*, pages 263–268. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Chen:2021:DVR**

[CWD+21] Jiarong Chen, Zixin Wang, Yingfeng Ding, Haopeng Feng, and Dihu Chen. Design and verification of RISC-V CPU based on HLS and UVM. In IEEE, editor, *2021 IEEE International Conference on Computer Science, Electronic Information Engineering and Intelligent Control Technology (CEI)*, pages 659–664. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Chen:2024:RVC**

[CWS+24] Yuxing Chen, Xinrui Wang, Suwen Song, Lang Feng, and Zhongfeng Wang. RISC-V custom instructions of elementary functions for IoT endpoint devices. *IEEE Transactions on Computers*, 73(2):523–535, February 2024. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Chen:2020:XCM**

[CXL+20a] Chen Chen, Xiaoyan Xiang, Chang Liu, Yunhai Shang, Ren Guo, Dongqi Liu, Yimin Lu, Ziyi Hao, Jiahui Luo, Zhijian Chen, Chunqiang Li, Yu Pu, Jianyi Meng, Xiaolang Yan, Yuan Xie, and Xiaoning Qi. Xuantie-910: a commercial multi-core 12-stage pipeline out-of-order 64-bit high performance RISC-V processor with vector extension: Industrial product. In IEEE, editor, *2020 ACM/IEEE 47th Annual International Symposium on Computer Architecture (ISCA)*, pages 52–64. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Chen:2020:XIC**

[CXL+20b] Chen Chen, Xiaoyan Xiang, Chang Liu, Yunhai Shang, Ren Guo, Dongqi Liu, Yimin Lu, Ziyi Hao, Jiahui Luo, Zhijjan Chen, Chunqiang Li, Yu Pu, Jianyi Meng, Xiaolang Yan, Yuan Xie, and Xiaoning Qi. Xuantie-910: Innovating cloud and edge computing by RISC-V. In IEEE, editor, *Proceedings of the IEEE Hot Chips 32 Symposium (HCS), August, 2020*, pages 1–19. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020. URL `https://ieeexplore.ieee.org/document/9220630`.

**Cai:2022:RPT**

[CXLL22] Boyang Cai, Shaobin Xie, Quanyi Liang, and Wanying Lu. Research on penetration testing of IoT gateway based on RISC-V. In IEEE, editor, *2022 International Symposium on Advances in Informatics, Electronics and Education (ISAIEE)*, pages 422–425. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Chen:2022:RVS**

[CYJ+22] Chen Chen, Qimin Yuan, Xiaowen Jiang, Kai Huang, Peng Li, and Wei Xi. A RISC-V System-on-Chip based on dual-core isolation for smart grid security. In IEEE, editor, *2022 IEEE 6th Conference on Energy Internet and Energy System Integration (EI2)*, pages 1278–1283. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Gewehr:2023:IEC**

[dAGM23] Carlos Gabriel de Araujo Gewehr and Fernando Gehm Moraes. Improving the efficiency of cryptography algorithms on resource-constrained embedded systems via RISC-V instruction set extensions. In IEEE, editor, *2023 36th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Dao:2020:FRV**

[DAHK20] Nguyen Dao, Andrew Attwood, Bea Healy, and Dirk Koch. FlexBex: a RISC-V with a reconfigurable instruction extension. In IEEE, editor, *2020 International Conference on Field-Programmable Technology (ICFPT)*, pages 190–195. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Dorflinger:2021:CSO**

[DAK+21] A. Dörflinger, M. Albers, B. Kleinbeck, Y. Guan, H. Michalik, R. Klink, C. Blochwitz, A. Nechi, and M. Berekovic. A comparative survey of open-source application-class RISC-V processor implementations. In ACM, editor, *CF '21: Proceedings of the 18th ACM International Conference on Computing Frontiers, May 2021*, pages 12–20. ACM Press, New York, NY 10036, USA, 2021. ISBN 1-4503-8404-8. URL `https://dl.acm.org/doi/10.1145/3457388.3458657`.

**Dogan:2019:ASU**

[DAKK19] Halit Dogan, Masab Ahmad, Brian Kahne, and Omer Khan. Accelerating synchronization using moving compute to data model at 1,000-core multicore scale. *ACM Transactions on Architecture and Code Optimization*, 16(1): 4:1–4:??, March 2019. CODEN ???? ISSN 1544-3566 (print), 1544-3973 (electronic).

**DeSio:2021:SEH**

[DAPS21] Corrado De Sio, Sarah Azimi, Andrea Portaluri, and Luca Sterpone. SEU evaluation of hardened-by-replication software in RISC-V soft processor. In IEEE, editor, *2021 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**De:2019:FFI**

[DBGJ19] Asmit De, Aditya Basu, Swaroop Ghosh, and Trent Jaeger. FIXER: Flow integrity extensions for embedded RISC-V. In IEEE, editor, *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 348–353. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**De:2020:HAB**

[DBGJ20] Asmit De, Aditya Basu, Swaroop Ghosh, and Trent Jaeger. Hardware assisted buffer protection mechanisms for embedded RISC-V. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 39(12):4453–4465, 2020. CODEN ITCSDI. ISSN 0278-0070 (print), 1937-4151 (electronic).

**Dave:2021:CLA**

[DBP21] Avani Dave, Nilanjan Banerjee, and Chintan Patel. CARE: Lightweight attack resilient secure boot architecture with onboard recovery for RISC-V based SOC. In IEEE, editor, *2021 22nd International Symposium on Quality Electronic Design (ISQED)*, pages 516–521. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Doblas:2023:SAS**

[DCC+23] Max Doblas, Gerard Candón, Xavier Carril, Marc Domínguez, Enric Erra, Alberto González, César Hernández, Víctor Jiménez, Vatistas Kostalampros, Rubén Langarita,

Neiel Leyva, Guillem López-Paradís, Jonnatan Mendoza, Josep Oltra, Julián Pavón, Cristóbal Ramírez, Narcís Rodas, Enrico Reggiani, Mario Rodríguez, Carlos Rojas, Abraham Ruiz, Hugo Safadi, Víctor Soria, Alejandro Suanes, Iván Vargas, Fernando Arreza, Roger Figueras, Pau Fontova-Musté, Joan Marimon, Ricardo Martínez, Sergio Moreno, Jordi Sacristán, Oscar Alonso, Xavier Aragonés, Adrián Cristal, Ángel Diéguez, Manuel López, Diego Mateo, Francesc Moll, Miquel Moretó, Oscar Palomar, Marco A. Ramírez, Francesc Serra-Graells, Nehir Sonmez, Lluís Terés, Osman Unsal, Mateo Valero, and Luis Villa. Sargantana: an academic SoC RISC-V processor in 22nm FDSOI technology. In IEEE, editor, *2023 38th Conference on Design of Circuits and Integrated Systems (DCIS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Delshadtehrani:2021:SSP**

[DCEJ21] Leila Delshadtehrani, Sadullah Canakci, Manuel Egele, and Ajay Joshi. SealPK: Sealable protection keys for RISC-V. In IEEE, editor, *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1278–1281. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Ducasse:2023:JCS**

[DCL23] Quentin Ducasse, Pascal Cotret, and Loïc Lagadec. JIT compiler security through low-cost RISC-V extension. In IEEE, editor, *2023 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*, pages 125–128. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Deb:2023:RVS**

[DCM23] Suman Deb, Anupam Chattopadhyay, and Avi Mendelson. A RISC-V SoC with hardware trojans: Case study on trojan-ing the on-chip protocol conversion. In IEEE, editor, *2023 IFIP/IEEE 31st International Conference on Very Large Scale Integration (VLSI-SoC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Desalphine:2020:NMV**

[DDM+20] Vivian Desalphine, Somya

Dashora, Laxita Mali, K. Suhas, Aneesh Raveendran, and David Selvakumar. Novel method for verification and performance evaluation of a non-blocking level-1 instruction cache designed for out-of-order RISC-V superscaler processor on FPGA. In IEEE, editor, *2020 24th International Symposium on VLSI Design and Test (VDAT)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Ditzel:2021:AMR**

[DEA+21] Dave Ditzel, Roger Espasa, Nivard Aymerich, Allen Baum, Tom Berg, Jim Burr, Eric Hao, Jayesh Iyer, Miquel Izquierdo, Shankar Jayaratnam, Darren Jones, Chris Klingner, Jin Kim, Stephen Lee, Marc Lupon, Grigorios Magklis, Bojan Maric, Rajib Nath, Mike Neilly, Duane Northcutt, Bill Orner, Jose Renau, Gerard Reves, Xavier Reves, Tom Riordan, Pedro Sanchez, Sri Samudrala, Guillem Sole, Raymond Tang, Tommy Thorn, Francisco Torres, Sebastia Tortella, and Daniel Yau. Accelerating ML recommendation with over a thousand RISC-V/Tensor processors on Esperanto's ET-SoC-1 chip. In IEEE, editor, *2021 IEEE Hot Chips 33 Symposium (HCS)*, pages 1–23. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Delshadtehrani:2018:NPM**

[DEC+18] Leila Delshadtehrani, Schuyler Eldridge, Sadullah Canakci, Manuel Egele, and Ajay Joshi. Nile: a programmable monitoring coprocessor. *IEEE Computer Architecture Letters*, 17(1):92–95, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

**Dupuis:2023:SCR**

[DFA+23] Théo Dupuis, Yoan Fournier, MohammadHossein AskariHemmat, Nizar El Zarif, François Leduc-Primeau, Jean Pierre David, and Yvon Savaria. Sparq: a custom RISC-V vector processor for efficient sub-byte quantized inference. In IEEE, editor, *2023 21st IEEE Interregional NEWCAS Conference (NEWCAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**De:2022:HSU**

[DG22] Asmit De and Swaroop Ghosh. HeapSafe: Securing unprotected heaps in

RISC-V. In IEEE, editor, *2022 35th International Conference on VLSI Design and 2022 21st International Conference on Embedded Systems (VLSID)*, pages 120–125. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Duran:2017:SCP**

[DGA+17] Ckristian Duran, Luis E. Rueda G., Andres Amaya, Rolando Torres, Javier Ardila, Luis Rueda D., Giovanny Castillo, Anderson Agudelo, Camilo Rojas, Luis Chaparro, Harry Hurtado, Juan Romero, Wilmer Ramirez, Hector Gomez, Hugo Hernandez, and Elkim Roa. A system-on-chip platform for the Internet of Things featuring a 32-bit RISC-V based microcontroller. In IEEE, editor, *2017 IEEE 8th Latin American Symposium on Circuits & Systems (LASCAS)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017.

**DeMulder:2019:IPR**

[DGH19] Elke De Mulder, Samatha Gummalla, and Michael Hutter. INVITED: Protecting RISC-V against side-channel attacks. In IEEE, editor, *2019 56th ACM/IEEE Design Automation Conference (DAC)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Dao:2021:CPA**

[DHL+21] Ba-Anh Dao, Trong-Thuc Hoang, Anh-Tien Le, Akira Tsukamoto, Kuniyasu Suzaki, and Cong-Kha Pham. Correlation power analysis attack resisted cryptographic RISC-V SoC with random dynamic frequency scaling countermeasure. *IEEE Access*, 9:151993–152014, 2021. ISSN 2169-3536.

**Doran:2023:EVR**

[DK23] Michael A. Doran and Nabeeh Kandalaft. Embedded virtualization on RISC-V with seL4. In IEEE, editor, *2023 IEEE 14th Annual Ubiquitous Computing, Electronics & Mobile Communication Conference (UEMCON)*, pages 0736–0740. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Dorflinger:2022:FFT**

[DKA+22] Alexander Dörflinger, Benedikt Kleinbeck, Mark Albers, Harald Michalik, and Martin Moya. A framework for fault tolerance in RISC-V. In IEEE, editor, *2022*

*IEEE Intl Conf on Dependable, Autonomic and Secure Computing, Intl Conf on Pervasive Intelligence and Computing, Intl Conf on Cloud and Big Data Computing, Intl Conf on Cyber Science and Technology Congress (DASC/PiCom/CBDCom/CyberSciTech)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**DiGirolamo:2021:RVN**

[DKC+21] Salvatore Di Girolamo, Andreas Kurth, Alexandru Calotoiu, Thomas Benz, Timo Schneider, Jakub Beránek, Luca Benini, and Torsten Hoefler. A RISC-V in-network accelerator for flexible high-performance low-power packet processing. In IEEE, editor, *2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture (ISCA)*, pages 958–971. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Dimitrakopoulos:2023:MAB**

[DKT+23] G. Dimitrakopoulos, E. Kallitsounakis, Z. Takakis, A. Stefanidis, and C. Nicopoulos. Multi-armed bandits for autonomous test application in RISC-V processor verification. In IEEE, editor, *2023 12th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Dietrich:2017:OVA**

[DL17] Christian Dietrich and Daniel Lohmann. OSEK-V: application-specific RTOS instantiation in hardware. *ACM SIGPLAN Notices*, 52 (4):111–120, May 2017. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

**Dow:2021:SHS**

[DLMP21] Hsu-Kang Dow, Tuo Li, William Miles, and Sri Parameswaran. SHORE: Hardware/software method for memory safety acceleration on RISC-V. In IEEE, editor, *2021 58th ACM/IEEE Design Automation Conference (DAC)*, pages 289–294. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Duran:2020:SFB**

[DMR+20] Ckristian Duran, Hanssel Morales, Camilo Rojas, Annachiara Ruospo, Ernesto Sanchez, and Elkim Roa.

Simulation and formal: The best of both domains for instruction set verification of RISC-V based processors. In IEEE, editor, *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Dang:2024:RAO**

[DNKDN+24] Tuan-Kiet Dang, Khai-Duy Nguyen, Binh Kieu-Do-Nguyen, Trong-Thuc Hoang, and Cong-Kha Pham. Realization of authenticated one-pass key establishment on RISC-V micro-controller for IoT applications. *Future Internet*, 16(5):157, May 3, 2024. CODEN ???? ISSN 1999-5903. URL `https://www.mdpi.com/1999-5903/16/5/157`.

**Dao:2023:HTC**

[DNN23] Ba-Anh Dao, Ngoc-Quynh Nguyen, and Chung-Tien Nguyen. A high-throughput and compact GOST-28147-89 accelerator for RISC-V System-on-Chip. In IEEE, editor, *2023 15th International Conference on Knowledge and Systems Engineering (KSE)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**deOliveira:2023:EFT**

[dOK23] Ádria Barros de Oliveira and Fernanda Lima Kastensmidt. Evaluating fault-tolerant techniques on COTS RISC-V NOEL-V processor in Zynq UltraScale+ FPGA under proton testing. *IEEE Transactions on Nuclear Science*, 70(8): 1708–1715, 2023. CODEN IRNSAM. ISSN 0018-9499 (print), 1558-1578 (electronic).

**DosReis:2019:RVA**

[Dos19] Anthony J. Dos Reis. *RISC-V Assembly Language*. ????, ????, 2019. ISBN 1-0884-6200-6. v + 149 pp. LCCN QA76.9.A73 D67 2019.

**deOliveira:2020:ESC**

[dOTB+20] Ádria B. de Oliveira, Lucas A. Tambara, Fabio Benevenuti, Luis A. C. Benites, Nemitala Added, Vitor A. P. Aguiar, Nilberto H. Medina, Marcilei A. G. Silveira, and Fernanda L. Kastensmidt. Evaluating soft core RISC-V processor in SRAM-based FPGA under radiation effects. *IEEE Transactions on Nuclear Science*, 67(7):1503–1510, 2020. CODEN IRNSAM. ISSN 0018-9499 (print), 1558-1578 (electronic).

**Dharsni:2022:OHF**

[DPP22] I Thanga Dharsni, Kirti S.

Pande, and Manoj Kumar Panda. Optimized hazard free pipelined architecture block for RV32I RISC-V processor. In IEEE, editor, *2022 3rd International Conference on Smart Electronics and Communication (ICOSEC)*, pages 739–746. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Dennis:2017:SCR**

[DPV+17] Don Kurian Dennis, Ayushi Priyam, Sukhpreet Singh Virk, Sajal Agrawal, Tanuj Sharma, Arijit Mondal, and Kailash Chandra Ray. Single cycle RISC-V micro architecture processor and its FPGA prototype. In IEEE, editor, *2017 7th International Symposium on Embedded Computing and System Design (ISED)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017.

**Duran:2016:BRV**

[DRC+16] Ckristian Duran, D. Luis Rueda, Giovanny Castillo, Anderson Agudelo, Camilo Rojas, Luis Chaparro, Harry Hurtado, Juan Romero, Wilmer Ramirez, Hector Gomez, Javier Ardila, Luis Rueda, Hugo Hernandez, Jose Amaya, and Elkim Roa. A 32-bit RISC-V AXI4-lite bus-based microcontroller with 10-bit SAR ADC. In IEEE, editor, *2016 IEEE 7th Latin American Symposium on Circuits & Systems (LASCAS)*, pages 315–318. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2016.

**Domingos:2023:SRV**

[DRN+23] Joao Mario Domingos, Tiago Rocha, Nuno Neves, Nuno Roma, Pedro Tomás, and Leonel Sousa. Supporting RISC-V performance counters through Linux performance analysis tools. In IEEE, editor, *2023 IEEE 34th International Conference on Application-specific Systems, Architectures and Processors (ASAP): ASAP 2023, 19–21 July 2023, Porto, Portugal*, pages 94–101. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, July 2023.

**Ditzel:2022:AMR**

[DtEt22] David R. Ditzel and the Esperanto team. Accelerating ML recommendation with over 1,000 RISC-V/Tensor processors on Esperanto's ET-SoC-1 chip. *IEEE Micro*, 42(3):31–38, May/June 2022. CODEN IEMIDZ. ISSN 0272-1732

(print), 1937-4143 (electronic).

**Das:2019:SMR**

[DUM+19] S. Das, R. H. Unnithan, A. Menon, C. Rebeiro, and K. Veezhinathan. SHAKTI-MS: a RISC-V processor for memory safety in C. In Jian-Jia Chen and Aviral Shrivastava, editors, *LCTES '19: 20th ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems. Phoenix, AZ, USA. 23 June 2019*, pages 19–32. ACM Press, New York, NY 10036, USA, 2019. ISBN 1-4503-6724-0. URL `https://dl.acm.org/doi/10.1145/3316482.3326356`.

**Duran:2020:EER**

[DWG+20] Ckristian Duran, Megan Wachs, Luis E. Rueda G., Albert Huntington, Javier Ardila, Jack Kang, Andres Amaya, Hector Gomez, Juan Romero, Laude Fernandez, Felipe Flechas, Rolando Torres, Juan Moya, Wilmer Ramirez, Julian Arenas, Juan Gomez, Hanssel Morales, Camilo Rojas, Alex Mantilla, Elkim Roa, and Krste Asanovic. An energy-efficient RISC-V RV32IMAC microcontroller for periodical-driven sensing applications. In IEEE, editor, *2020 IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Davidson:2018:COS**

[DXT+18] Scott Davidson, Shaolin Xie, Christopher Torng, Khalid Al-Hawai, Austin Rovinski, Tutu Ajayi, Luis Vega, Chun Zhao, Ritchie Zhao, Steve Dai, Aporva Amarnath, Bandhav Veluri, Paul Gao, Anuj Rao, Gai Liu, Rajesh K. Gupta, Zhiru Zhang, Ronald Dreslinski, Christopher Batten, and Michael Bedford Taylor. The Celerity open-source 511-core RISC-V tiered accelerator fabric: Fast architectures and design methodologies for fast chips. *IEEE Micro*, 38(2): 30–41, March/April 2018. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `https://www.computer.org/csdl/mags/mi/2018/02/mmi2018020030-abs.html`.

**Dong:2019:SSE**

[DXYZ19] Jiajie Dong, Long Xi, Mengxi Yu, and Zeming Zhang. Software simulation error injection in RAM on RISC-V of PolarFire FPGA. In IEEE, editor, *2019 IEEE 19th International Conference on*

*Software Quality, Reliability and Security Companion (QRS-C)*, pages 499–502. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Deng:2022:DSH**

[DYZ+22] Junyong Deng, Zekun Ye, Kai Zhou, Xiaoliang Fu, Baoxiang Zhang, and Xiaoyan Xie. Design of software–hardware collaborative graph computing accelerator based on RISC-V. In IEEE, editor, *2022 7th International Conference on Integrated Circuits and Microsystems (ICICM)*, pages 404–410. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Ding:2023:DIS**

[DZZZ23] Can Ding, Yunfei Zhu, Rongcai Zhao, and Xiao Zhang. Design and implementation of a speech recognition module based on RISC-V embedded processor. In IEEE, editor, *2023 8th International Conference on Intelligent Computing and Signal Processing (ICSP)*, pages 20–27. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Eassa:2019:RVB**

[EAI19] Hossameldin Eassa, Ihab Adly, and Hanady H. Issa. RISC-V based implementation of programmable logic controller on FPGA for industry 4.0. In IEEE, editor, *2019 31st International Conference on Microelectronics (ICM)*, pages 98–102. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Ecker:2022:SRV**

[EAM+22] Wolfgang Ecker, Peer Adelt, Wolfgang Mueller, Reinhold Heckmann, Milos Krstic, Vladimir Herdt, Rolf Drechsler, Gerhard Angst, Ralf Wimmer, Andreas Mauderer, Rafael Stahl, Karsten Emrich, Daniel Mueller-Gritschneder, Bernd Becker, Philipp Scholl, Eyck Jentzsch, Jan Schlamelcher, Kim Grüttner, Paul Palomero Bernardo, Oliver Bringmann, Mihaela Damian, Julian Oppermann, Andreas Koch, Jörg Bormann, Johannes Partzsch, Christian Mayr, and Wolfgang Kunz. The Scale4Edge RISC-V ecosystem. In IEEE, editor, *2022 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 808–813. IEEE Computer Society Press, 1109 Spring Street, Suite 300,

Silver Spring, MD 20910, USA, 2022.

**Elkhatib:2021:ARV**

[EAMK21] Rami Elkhatib, Reza Azarderakhsh, and Mehran Mozaffari-Kermani. Accelerated RISC-V for SIKE. In IEEE [IEE21], pages 131–138. ISBN 1-66542-293-9 (print), 1-66544-648-X (e-book). LCCN ????

**Elmohr:2018:RFG**

[EEI+18] Mahmoud A. Elmohr, Ahmed S. Eissa, Moamen Ibrahim, Mostafa Khamis, Sameh El-Ashry, Ahmed Shalaby, Mohamed AbdElsalam, and M. Watheq El-Kharashi. RVNoC: a framework for generating RISC-V NoC-Based MPSoC. In IEEE, editor, *2018 26th Euromicro International Conference on Parallel, Distributed and Network-based Processing (PDP)*, pages 617–621. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Eni:2022:EHB**

[EGBS22] Yossi Eni, Shlomo Greenberg, and Yehuda Ben-Shimol. Efficient hint-based event (EHE) issue scheduling for hardware multithreaded RISC-V pipeline. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 69(2):735–745, 2022. ISSN 1549-8328 (print), 1558-0806 (electronic).

**Eckert:2020:UTI**

[EHK20] Marcel Eckert, Jan Haase, and Bernd Klauer. Unifying timer and interrupt management for an ARM-RISC-V-Heterogeneous multicore. In IEEE, editor, *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, pages 2302–2309. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Emil:2023:DEA**

[EHN23] Demyana Emil, Mohammed Hamdy, and Gihan Nagib. Development an efficient AXI-interconnect unit between set of customized peripheral devices and an implemented dual-core RISC-V processor. *The Journal of Supercomputing*, 79(15): 17000–17019, October 2023. CODEN JOSUED. ISSN 0920-8542 (print), 1573-0484 (electronic). URL `https://link.springer.com/article/10.1007/s11227-023-05304-1`.

**Elkhatib:2022:ARV**

[EKAK22] Rami Elkhatib, Brian Koziel, Reza Azarderakhsh, and Mehran Mozaffari Kermani. Accelerated RISC-V for

post-quantum SIKE. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 69(6):2490–2501, 2022. ISSN 1549-8328 (print), 1558-0806 (electronic).

**Elmohr:2020:EFI**

[ELG20] Mahmoud A. Elmohr, Haohao Liao, and Catherine H. Gebotys. EM fault injection on ARM and RISC-V. In IEEE, editor, *2020 21st International Symposium on Quality Electronic Design (ISQED)*, pages 206–212. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Eggimann:2019:RVB**

[EMMB19] Manuel Eggimann, Stefan Mach, Michele Magno, and Luca Benini. A RISC-V based open hardware platform for always-on wearable smart sensing. In IEEE, editor, *2019 IEEE 8th International Workshop on Advances in Sensors and Interfaces (IWASI)*, pages 169–174. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Eliahu:2021:MME**

[ERGK21] Adi Eliahu, Ronny Ronen, Pierre-Emmanuel Gaillardon, and Shahar Kvatinsky. multiPULPly: a multiplication engine for accelerating neural networks on ultra-low-power architectures. *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, 17(2):24:1–24:27, April 2021. CODEN ???? ISSN 1550-4832 (print), 1550-4840 (electronic). URL `https://dl.acm.org/doi/10.1145/3432815`.

**Elsadek:2021:RVR**

[ET21] Islam Elsadek and Eslam Yahya Tawfik. RISC-V resource-constrained cores: a survey and energy comparison. In IEEE, editor, *2021 19th IEEE International New Circuits and Systems Conference (NEWCAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Elsabbagh:2020:VOC**

[ETR+20] Fares Elsabbagh, Blaise Tine, Priyadarshini Roshan, Ethan Lyons, Euna Kim, Da Eun Shim, Lingjun Zhu, Sung Kyu Lim, and Hyesoon Kim. Vortex: OpenCL compatible RISC-V GPGPU. *arXiv.org*, ?? (??):1–7, February 27, 2020. URL `https://arxiv.org/abs/2002.12151`.

**Funck:2023:IIL**

[FAPHD23] Milan Funck, Sallar Ahmadi-

Pour, Vladimir Herdt, and Rolf Drechsler. Identification of ISA-level mutation-classes for qualification of RISC-V formal verification. In IEEE, editor, *2023 Forum on Specification & Design Languages (FDL)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Furano:2022:ERL**

[FDMM22] Gianluca Furano, Stefano Di Mascio, Alessandra Menicucci, and Claudio Monteleone. A European roadmap to leverage RISC-V in space applications. In IEEE, editor, *2022 IEEE Aerospace Conference (AERO)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Fernandes:2023:EAS**

[FdRES23] João Cassiano V. Fernandes, Helbert da Rocha, and António Espírito-Santo. Encryption and authentication in smart transducers implemented in RISC-V soft-core processors. In IEEE, editor, *2023 IEEE International Conference on Industrial Technology (ICIT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Faller:2023:CBA**

[FDS+23] Tobias Faller, Nikolaos I. Deligiannis, Markus Schwörer, Matteo Sonza Reorda, and Bernd Becker. Constraint-based automatic SBST generation for RISC-V processor families. In IEEE, editor, *2023 IEEE European Test Symposium (ETS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Felzmann:2020:RCA**

[FFW20] Isaías Felzmann, João Fabrício Filho, and Lucas Wanner. Risk-5: Controlled approximations for RISC-V. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 39 (11):4052–4063, 2020. CODEN ITCSDI. ISSN 0278-0070 (print), 1937-4151 (electronic).

**Fiolhais:2019:LEH**

[FGD+19] Luís Fiolhais, Fernando Gonçalves, Rui P. Duarte, Mário Véstias, and Jose T. de Sousa. Low energy heterogeneous computing with multiple RISC-V and CGRA cores. In IEEE, editor, *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5. IEEE Computer

Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Funck:2022:VPD**

[FHD22] Milan Funck, Vladimir Herdt, and Rolf Drechsler. Virtual prototype driven design, implementation and evaluation of RISC-V instruction set extensions. In IEEE, editor, *2022 25th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, pages 14–19. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Feng:2022:RRV**

[FHL+22] Lang Feng, Jiayi Huang, Luyi Li, Haochen Zhang, and Zhongfeng Wang. RvDfi: a RISC-V architecture with security enforcement by high performance complete data-flow integrity. *IEEE Transactions on Computers*, 71(10):2499–2512, October 2022. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Farshchi:2019:IND**

[FHY19] Farzad Farshchi, Qijing Huang, and Heechul Yun. Integrating NVIDIA deep learning accelerator (NVDLA) with RISC-V SoC on FireSim. In IEEE, editor, *2019 2nd Workshop on Energy Efficient Machine Learning and Cognitive Computing for Embedded Applications (EMC2)*, pages 21–25. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**FernandesDosSantos:2022:EEN**

[FKS22] Fernando Fernandes Dos Santos, Angeliki Kritikakou, and Olivier Sentieys. Experimental evaluation of neutron-induced errors on a multicore RISC-V platform. In IEEE, editor, *2022 IEEE 28th International Symposium on On-Line Testing and Robust System Design (IOLTS)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Flamand:2018:GRV**

[FRC+18] Eric Flamand, Davide Rossi, Francesco Conti, Igor Loi, Antonio Pullini, Florent Rotenberg, and Luca Benini. GAP-8: a RISC-V SoC for AI at the edge of the IoT. In IEEE, editor, *2018 IEEE 29th International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pages 1–4. IEEE Computer So-

ciety Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Fritzmann:2019:TRS**

[FSMG+19] Tim Fritzmann, Uzair Sharif, Daniel Müller-Gritschneder, Cezar Reinbrecht, Ulf Schlichtmann, and Johanna Sepulveda. Towards reliable and secure post-quantum co-processors based on RISC-V. In IEEE, editor, *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1148–1153. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Forno:2021:CEN**

[FSMU21] Evelina Forno, Andrea Spitale, Enrico Macii, and Gianvito Urgese. Configuring an embedded neuromorphic coprocessor using a RISC-V chip for enabling edge computing applications. In IEEE, editor, *2021 IEEE 14th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC)*, pages 328–332. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Faller:2021:TSB**

[FSPB21] Tobias Faller, Philipp Scholl, Tobias Paxian, and Bernd Becker. Towards SAT-based SBST generation for RISC-V cores. In IEEE, editor, *2021 IEEE 22nd Latin American Test Symposium (LATS)*, pages 1–2. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Fritzmann:2020:ERV**

[FSS20] Tim Fritzmann, Georg Sigl, and Johanna Sepúlveda. Extending the RISC-V instruction set for hardware acceleration of the post-quantum scheme LAC. In IEEE, editor, *2020 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1420–1425. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Fibich:2020:EOS**

[FTRH20] Christian Fibich, Stefan Tauner, Peter Rössler, and Martin Horauer. Evaluation of open-source linear algebra libraries targeting ARM and RISC-V architectures. In IEEE, editor, *2020 15th Conference on Computer Science and Information Systems (FedCSIS)*, pages 663–672. IEEE Com-

puter Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Forlin:2023:URV**

[FvHC+23] Bruno Endres Forlin, Wouter van Huffelen, Carlo Cazzaniga, Paolo Rech, Nikolaos Alachiotis, and Marco Ottavi. An unprotected RISC-V soft-core processor on an SRAM FPGA: Is it as bad as it sounds? In IEEE, editor, *2023 IEEE European Test Symposium (ETS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Feng:2019:ILN**

[FWZL19] Shanggong Feng, Junning Wu, Shengang Zhou, and Renwei Li. The implementation of LeNet-5 with NVDLA on RISC-V SoC. In IEEE, editor, *2019 IEEE 10th International Conference on Software Engineering and Service Science (ICSESS)*, pages 39–42. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Gobieski:2023:MMM**

[GAE+23] Graham Gobieski, Oguz Atli, Cagri Erbagci, Ken Mai, Nathan Beckmann, and Brandon Lucia. MANIC: a $19\mu W$ @ 4MHz, 256 MOPS/mW, RISC-V microcontroller with embedded MRAM main memory and vector-dataflow coprocessor in 22nm bulk finFET CMOS. In IEEE, editor, *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Geier:2023:CCA**

[GAMG+23] Johannes Geier, Lukas Auer, Daniel Mueller-Gritschneder, Uzair Sharif, and Ulf Schlichtmann. CompaSeC: a compiler-assisted security countermeasure to address instruction skip fault attacks on RISC-V. In IEEE, editor, *2023 28th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Gholizadehazari:2021:FIR**

[GAO21] Erfan Gholizadehazari, Tuba Ayhan, and Berna Ors. An FPGA implementation of a RISC-V based SoC system for image processing applications. In IEEE, editor, *2021 29th Signal Processing and Communications Appli-*

*cations Conference (SIU)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Gaurav:2021:DIL**

[GBP21] Tanya Gaurav, Amit Bhatt, and Rutu Parekh. Design and implementation of low power RISC V ISA based coprocessor design for matrix multiplication. In IEEE, editor, *2021 Second International Conference on Electronics and Sustainable Communication Systems (ICESC)*, pages 189–195. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Gruin:2021:SET**

[GCCR21] Alban Gruin, Thomas Carle, Hugues Cassé, and Christine Rochange. Speculative execution and timing predictability in an open source RISC-V core. In IEEE, editor, *2021 IEEE Real-Time Systems Symposium (RTSS)*, pages 393–404. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Gao:2023:DGC**

[GCL+23] Fei Gao, Ting-Jung Chang, Ang Li, Marcelo Orenes-Vera, Davide Giri, Paul J. Jackson, August Ning, Georgios Tziantzioulis, Joseph Zuckerman, Jinzheng Tu, Kaifeng Xu, Grigory Chirkov, Gabriele Tombesi, Jonathan Balkind, Margaret Martonosi, Luca Carloni, and David Wentzlaff. DECADES: a 67mm2, 1.46TOPS, 55 giga cache-coherent 64-bit RISC-V instructions per second, heterogeneous many-core SoC with 109 tiles including accelerators, intelligent storage, and eFPGA in 12nm FinFET. In IEEE, editor, *2023 IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–2. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Gruin:2023:MTP**

[GCR+23] Alban Gruin, Thomas Carle, Christine Rochange, Hugues Cassé, and Pascal Sainrat. MINOTAuR: a timing predictable RISC-V core featuring speculative execution. *IEEE Transactions on Computers*, 72 (1):183–195, January 2023. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Gustafson:2019:PCN**

[GD19] John Gustafson and Vassil Dimitrov, editors. *Proceedings of the Conference for*

*Next Generation Arithmetic 2019, Singapore, March 2019*, ICPS. ACM Press, New York, NY 10036, USA, 2019. ISBN 1-4503-7139-6. LCCN ????

**Gava:2022:SEA**

[GDR+22] Jonas Gava, Guilherme Dorneles, Ricardo Reis, Rafael Garibotti, and Luciano Ost. Soft error assessment of CNN inference models running on a RISC-V processor. In IEEE, editor, *2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Genkina:2024:NOS**

[Gen24] Dina Genkina. News: Open-source hardware secures a win: sprung from RISC-V's roots, the first open security chip hits the market. *IEEE Spectrum*, 61 (4):6–13, April 2024. CODEN IEESAM. ISSN 0018-9235 (print), 1939-9340 (electronic).

**Guthmuller:2024:XRV**

[GFB+24] Eric Guthmuller, César Fuguet, Andrea Bocco, Jérôme Fereyre, Riccardo Alidori, Ihsane Tahir, and Yves Durand. Xvpfloat: RISC-V ISA extension for variable extended precision floating point computation. *IEEE Transactions on Computers*, 73(7):1683–1697, July 2024. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Ghosh:2018:TMT**

[GG18] Kunal Promode Ghosh and Anagha K. Ghosh. Technology mediated tutorial on RISC-V CPU core implementation and sign-off using revolutionary EDA management system (EMS) — VSDFLOW. In IEEE, editor, *2018 China Semiconductor Technology International Conference (CSTIC)*, pages 1–3. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Gonzalez-Gomez:2021:TGA**

[GGÁARG+21] Jeferson González-Gómez, Steven Ávila-Ardón, Jonathan Rojas-González, Andres Stephen-Cantillano, Jorge Castro-Godínez, Carlos Salazar-García, Muhammad Shafique, and Jörg Henkel. TailoredCore: Generating application-specific RISC-V-based cores. In IEEE, editor, *2021 IEEE 12th Latin America Symposium on Circuits and System (LASCAS)*, pages 1–4. IEEE Computer Society

Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Garzon:2022:RVB**

[GGH+22] Esteban Garzón, Roman Golman, Odem Harel, Tzachi Noy, Yehuda Kra, Asaf Pollock, Slava Yuzhaninov, Yonatan Shoshan, Yehuda Rudin, Yoav Weitzman, Marco Lanuzza, and Adam Teman. A RISC-V-based research platform for rapid design cycle. In IEEE, editor, *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 2614–2615. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Gupta:2023:CDR**

[GJC23] Naina Gupta, Arpan Jati, and Anupam Chattopadhyay. CRYSTALS-Dilithium on RISC-V processor: Lightweight secure boot using post-quantum digital signature. In IEEE, editor, *2023 IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Gerlin:2022:DTC**

[GKB+22] Nicolas Gerlin, Endri Kaja, Monideep Bora, Keerthikumara Devarajegowda, Dominik Stoffel, Wolfgang Kunz, and Wolfgang Ecker. Design of a tightly-coupled RISC-V physical memory protection unit for online error detection. In IEEE, editor, *2022 IFIP/IEEE 30th International Conference on Very Large Scale Integration (VLSI-SoC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Goud:2021:GAD**

[GLS21] B. Mahesh Goud, Dilip Lilaramani, and Mahendra Swain. Generation and authentication of digital certificates using Ethereum based decentralized mechanism for mitigating data fraud on RISC-V. In IEEE, editor, *2021 International Conference on Computational Performance Evaluation (ComPE)*, pages 905–909. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Gao:2021:EEF**

[GM21] Dapeng Gao and Tom Melham. End-to-end formal verification of a RISC-V processor extended with capability pointers. In IEEE, editor, *2021 Formal Methods in Computer Aided Design (FMCAD)*, pages 24–

33. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Moon:2019:RFS**

[gMCP19] Hyeon gyun Moon, Jeonghun Cho, and Daejin Park. Reconfigurable fault-safe processor platform based on RISC-V for large-scaled IoT-Driven applications. In IEEE, editor, *2019 IEEE Intl Conf on Dependable, Autonomic and Secure Computing, Intl Conf on Pervasive Intelligence and Computing, Intl Conf on Cloud and Big Data Computing, Intl Conf on Cyber Science and Technology Congress (DASC/PiCom/CBDCom/CyberSciTech)*, pages 627–632. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Gomez:2023:HLV**

[GMFC23] Constantino Gómez, Filippo Mantovani, Erich Focht, and Marc Casas. HPCG on long-vector architectures: Evaluation and optimization on NEC SX-Aurora and RISC-V. *Future Generation Computer Systems*, 143(??):152–162, June 2023. CODEN FGSEVI. ISSN 0167-739X (print), 1872-7115 (electronic). URL `http://www.sciencedirect.com/science/article/pii/S0167739X23000225`.

**Ghasemi:2023:SIH**

[GMK+23] S. Maryam Ghasemi, Sergej Meschkov, Jonas Krautter, Dennis R. E. Gnad, and Mehdi B. Tahoori. SLM ISA and hardware extensions for RISC-V processors. In IEEE, editor, *2023 IEEE 29th International Symposium on On-Line Testing and Robust System Design (IOLTS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Gao:2023:LSL**

[GMS+23] Yimin Gao, Sergiu Mosanu, Mohammad Nazmus Sakib, Vaibhav Verma, Xinfei Guo, and Mircea Stan. LiteAIR5: a system-level framework for the design and modeling of AI-extended RISC-V cores. In IEEE, editor, *2023 IEEE 36th International System-on-Chip Conference (SOCC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Gokulan:2020:DBD**

[GMV20] T Gokulan, Akshay Muraleedharan, and Kuruvilla Varghese. Design of a 32-bit, dual pipeline superscalar RISC-V processor on

FPGA. In IEEE, editor, *2020 23rd Euromicro Conference on Digital System Design (DSD)*, pages 340–343. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Gordon:2022:PKL**

[GPL22] Nicholas Gordon, Kevin Pedretti, and John R. Lange. Porting the Kitten lightweight kernel operating system to RISC-V. In IEEE, editor, *2022 IEEE/ACM International Workshop on Runtime and Operating Systems for Supercomputers (ROSS)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Garofalo:2022:DHRa**

[GPV+22] Angelo Garofalo, Matteo Perotti, Luca Valente, Yvan Tortorella, Alessandro Nadalini, Luca Benini, Davide Rossi, and Francesco Conti. Darkside: 2.6GFLOPS, 8.7mW heterogeneous RISC-V cluster for extreme-edge on-chip DNN inference and training. In IEEE, editor, *ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC)*, pages 273–276. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Gray:2016:GPM**

[Gra16] Jan Gray. GRVI Phalanx: a massively parallel RISC-V FPGA accelerator accelerator. In IEEE, editor, *2016 IEEE 24th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pages 17–20. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2016.

**Garofalo:2019:PNC**

[GRC+19] Angelo Garofalo, Manuele Rusci, Francesco Conti, Davide Rossi, and Luca Benini. PULP-NN: a computing library for quantized neural network inference at the edge on RISC-V based parallel ultra low power clusters. In IEEE, editor, *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pages 33–36. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Garcia-Ramirez:2020:SRV**

[GRCRCG+20] R. Garcia-Ramirez, A. Chacon-Rodriguez, R. Castro-Gonzalez, A. Arnaud, M. Miguez, J. Gak, R. Molina-Robles, G. Madrigal-Boza,

M. Oviedo-Hernandez, E. Solera-Bolanos, D. Salazar-Sibaja, D. Sanchez-Jimenez, M. Fonseca-Rodriguez, J. Arrieta-Solorzano, and R. Rimolo-Donadio. Siwa: a RISC-V RV32I based microcontroller for implantable medical applications. In IEEE, editor, *2020 IEEE 11th Latin American Symposium on Circuits & Systems (LASCAS)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Gorius:2022:DER**

[GRD22] Jean-Michel Gorius, Simon Rokicki, and Steven Derrien. Design exploration of RISC-V soft-cores through speculative high-level synthesis. In IEEE, editor, *2022 International Conference on Field-Programmable Technology (ICFPT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Greengard:2020:NWR**

[Gre20] Samuel Greengard. News: Will RISC-V revolutionize computing? *Communications of the Association for Computing Machinery*, 63(5):30–32, May 2020. CODEN CACMA2. ISSN 0001-0782 (print), 1557-7317 (electronic). URL `https://dl.acm.org/doi/abs/10.1145/3386377`.

**Gur:2018:FIB**

[GSDB18] Etki Gür, Zekiye Eda Sataner, Yusuf H. Durkaya, and Salih Bayar. FPGA implementation of 32-bit RISC-V processor with web-based assembler–disassembler. In IEEE, editor, *2018 International Symposium on Fundamentals of Electrical Engineering (ISFEE)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Gautschi:2017:NTR**

[GST+17] Michael Gautschi, Pasquale Davide Schiavone, Andreas Traber, Igor Loi, Antonio Pullini, Davide Rossi, Eric Flamand, Frank K. Gürkaynak, and Luca Benini. Near-threshold RISC-V core with DSP extensions for scalable IoT endpoint devices. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 25 (10):2700–2713, 2017. CODEN IEVSE9. ISSN 1063-8210 (print), 1557-9999 (electronic).

**Garofalo:2020:XAQ**

[GTC+20] Angelo Garofalo, Giuseppe Tagliavini, Francesco Conti, Davide Rossi, and Luca

Benini. XpulpNN: Accelerating quantized neural networks on RISC-V processors through ISA extensions. In IEEE, editor, *2020 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 186–191. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Garofalo:2021:XEEa**

[GTC+21a] Angelo Garofalo, Giuseppe Tagliavini, Francesco Conti, Luca Benini, and Davide Rossi. XpulpNN: Enabling energy efficient and flexible inference of quantized neural networks on RISC-V based IoT end nodes. In IEEE [IEE21], page 53. ISBN 1-66542-293-9 (print), 1-66544-648-X (e-book). LCCN ???? See [GTC+21b].

**Garofalo:2021:XEEb**

[GTC+21b] Angelo Garofalo, Giuseppe Tagliavini, Francesco Conti, Luca Benini, and Davide Rossi. XpulpNN: Enabling energy efficient and flexible inference of quantized neural networks on RISC-V based IoT end nodes. *IEEE Transactions on Emerging Topics in Computing*, 9(3): 1489–1505, July/September 2021. ISSN 2168-6750 (print), 2376-4562 (electronic). See [GTC+21b].

**Green:2021:TTI**

[GTCS21] Brad Green, Dillon Todd, Jon C. Calhoun, and Melissa C. Smith. TIGRA: a tightly integrated generic RISC-V accelerator interface. In IEEE, editor, *2021 IEEE International Conference on Cluster Computing (CLUSTER)*, pages 779–782. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Gousselot:2023:LCA**

[GTD+23] Théophile Gousselot, Olivier Thomas, Jean-Max Dutertre, Olivier Potin, and Jean-Baptiste Rigaud. Lightweight countermeasures against original linear code extraction attacks on a RISC-V core. In IEEE, editor, *2023 IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, pages 89–99. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Garofalo:2022:DHRb**

[GTP+22] Angelo Garofalo, Yvan Tortorella, Matteo Perotti, Luca Valente, Alessandro Nadalini, Luca Benini, Davide Rossi, and Francesco Conti. DARKSIDE: a heterogeneous RISC-V compute cluster for extreme-

edge on-chip DNN inference and training. *IEEE Open Journal of the Solid-State Circuits Society*, 2:231–243, 2022. ISSN 2644-1349.

**Gracia:2022:PTT**

[GVT+22] Darío Suárez Gracia, Alejandro Valero, Rubén Gran Tejero, María Villarroya, and Víctor Viñals. peRISCVcope: a tiny teaching-oriented RISC-V interpreter. In IEEE, editor, *2022 37th Conference on Design of Circuits and Integrated Circuits (DCIS)*, pages 01–06. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Gerlach:2023:SRM**

[GWZS23] Lukas Gerlach, Daniel Weber, Ruiyi Zhang, and Michael Schwarz. A security RISC: Microarchitectural attacks on hardware RISC-V CPUs. In IEEE, editor, *2023 IEEE Symposium on Security and Privacy (SP)*, pages 2321–2338. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Ge:2022:SDI**

[GXLW22] Zhilai Ge, Penghao Xiao, Mengxue Li, and Haipeng Wang. SoC design of intelligent recognition based on RISC-V. In IEEE, editor, *2022 International Conference on Automation, Robotics and Computer Engineering (ICARCE)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Guo:2023:TMS**

[GYW+23] Pengfei Guo, Yingjian Yan, Junjie Wang, Jingxin Zhong, Yanjiang Liu, and Jinsong Xu. Towards a metrics suite for evaluating cache side-channel vulnerability: Case studies on an open-source RISC-V processor. *Computers & Security*, 135(??):??, December 2023. CODEN CPSEDU. ISSN 0167-4048 (print), 1872-6208 (electronic). URL `http://www.sciencedirect.com/science/article/pii/S0167404823003905`.

**Gao:2022:RDR**

[GZ22] Jie Gao and Jun Zhang. Research and design of RISC-V four-stage out-of-order execution processor. In IEEE, editor, *2022 IEEE 16th International Conference on Solid-State & Integrated Circuit Technology (ICSICT)*, pages 1–3. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Gao:2022:TFI**

[GZC22] Zhanyuan Gao, Laiping Zhao, and Haonan Chen. A trigonometric function instruction set extension method based on RISC-V. In IEEE, editor, *2022 IEEE/ACIS 22nd International Conference on Computer and Information Science (ICIS)*, pages 119–126. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Gonzalez:2021:GWH**

[GZK+21] Abraham Gonzalez, Jerry Zhao, Ben Korpan, Hasan Genc, Colin Schmidt, John Wright, Ayan Biswas, Alon Amid, Farhana Sheikh, Anton Sorokin, Sirisha Kale, Mani Yalamanchi, Ramya Yarlagadda, Mark Flannigan, Larry Abramowitz, Elad Alon, Yakun Sophia Shao, Krste Asanović, and Borivoje Nikolić. A 16mm2 106.1 GOPS/W heterogeneous RISC-V multi-core multi-accelerator SoC in low-power 22nm FinFET. In IEEE, editor, *ESSCIRC 2021 — IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, pages 259–262. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Hadayeghparast:2022:HSP**

[HBSE22] Shahriar Hadayeghparast, Siavash Bayat-Sarmadi, and Shahriar Ebrahimi. High-speed post-quantum crypto-processor based on RISC-V architecture for IoT. *IEEE Internet of Things Journal*, 9(17):15839–15846, 2022. ISSN 2327-4662.

**Harb:2020:FPC**

[HC20] Hassan Harb and Cyrille Chavet. Fully parallel circular-shift rotation network for communication standards. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 67(12):3412–3416, December 2020. ISSN 1549-7747 (print), 1558-3791 (electronic). URL `https://ieeexplore.ieee.org/document/9099895`.

**Hung:2021:EEP**

[HCL+21] Yi-Wen Hung, Yao-Tse Chang, Shuenn-Yuh Lee, Chou-Ching Lin, and Gia-Shing Shieh. An energy-efficient and programmable RISC-V CNN coprocessor for real-time epilepsy detection and identification on wearable devices. In IEEE, editor, *2021 IEEE International Conference on Consumer Electronics — Taiwan (ICCE-TW)*, pages 1–2. IEEE Computer Society Press, 1109 Spring Street,

Suite 300, Silver Spring, MD 20910, USA, 2021.

**Harris:2021:RUR**

[HCP+21] Sarah L. Harris, Daniel Chaver, Luis Piñuel, J. I. Gomez-Perez, M. Hamza Liaqat, Zubair L. Kakakhel, Olof Kindgren, and Robert Owen. RVfpga: Using a RISC-V core targeted to an FPGA in computer architecture education. In IEEE, editor, *2021 31st International Conference on Field-Programmable Logic and Applications (FPL)*, pages 145–150. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**He:2023:ROS**

[HCW23] Tianchen He, Xiangning Chen, and Guokang Wang. Research on open source processor and analysis of current development dilemma based on RISC-V. In IEEE, editor, *2023 8th International Conference on Computer and Communication Systems (ICCCS)*, pages 768–774. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Hu:2021:AIS**

[HCZ21] Bowen Hu, Yun Chen, and Xiaoyang Zeng. An agile instruction set extension method based on the RISC-V processor. In IEEE, editor, *2021 IEEE 4th International Conference on Electronics Technology (ICET)*, pages 342–346. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Hoang:2020:CAT**

[HDT+20] Trong-Thuc Hoang, Ckristian Duran, Akira Tsukamoto, Kuniyasu Suzaki, and Cong-Kha Pham. Cryptographic accelerators for trusted execution environment in RISC-V processors. In IEEE, editor, *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Herdt:2019:SRV**

[HGD+19] Vladimir Herdt, Daniel Große, Rolf Drechsler, Christoph Gerum, Alexander Jung, Joscha-Joel Benz, Oliver Bringmann, Michael Schwarz, Dominik Stoffel, and Wolfgang Kunz. Systematic RISC-V based firmware design. In IEEE, editor, *2019 Forum for Specification and Design Languages (FDL)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street,

Suite 300, Silver Spring, MD 20910, USA, 2019.

**Herdt:2020:CRV**

[HGD20a] Vladimir Herdt, Daniel Große, and Rolf Drechsler. Closing the RISC-V compliance gap: Looking from the negative testing side. In IEEE, editor, *2020 57th ACM/IEEE Design Automation Conference (DAC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Herdt:2020:FAP**

[HGD20b] Vladimir Herdt, Daniel Große, and Rolf Drechsler. Fast and accurate performance evaluation for RISC-V using virtual prototypes. In IEEE, editor, *2020 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 618–621. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Herdt:2020:ECL**

[HGJD20] Vladimir Herdt, Daniel Große, Eyck Jentzsch, and Rolf Drechsler. Efficient cross-level testing for processor verification: a RISC-V case-study. In IEEE, editor, *2020 Forum for Specification and Design Languages (FDL)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Herdt:2018:ECR**

[HGLD18] Vladimir Herdt, Daniel Große, Hoang M. Le, and Rolf Drechsler. Extensible and configurable RISC-V based virtual prototype. In IEEE, editor, *2018 Forum on Specification & Design Languages (FDL)*, pages 5–16. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Herdt:2019:ECT**

[HGLD19] Vladimir Herdt, Daniel Große, Hoang M. Le, and Rolf Drechsler. Early concolic testing of embedded binaries with virtual prototypes: a RISC-V case study. In IEEE, editor, *2019 56th ACM/IEEE Design Automation Conference (DAC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Herdt:2020:RVB**

[HGPD20] Vladimir Herdt, Daniel Große, Pascal Pieper, and Rolf Drechsler. RISC-V based virtual prototype: An extensible and configurable platform for the system-level. *Journal of*

*Systems Architecture*, 109: 101756, 2020. CODEN JSARFB. ISSN 1383-7621 (print), 1873-6165 (electronic). URL `https://www.sciencedirect.com/science/article/pii/S1383762120300503`.

**Herdt:2020:ASV**

[HGTD20] Vladimir Herdt, Daniel Große, Sören Tempel, and Rolf Drechsler. Adaptive simulation with virtual prototypes for RISC-V: Switching between fast and accurate at runtime. In IEEE, editor, *2020 IEEE 38th International Conference on Computer Design (ICCD)*, pages 312–315. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Herdt:2021:ASV**

[HGTD21] Vladimir Herdt, Daniel Große, Sören Tempel, and Rolf Drechsler. Adaptive simulation with virtual prototypes in an open-source RISC-V evaluation platform. *Journal of Systems Architecture*, 116: 102135, 2021. CODEN JSARFB. ISSN 1383-7621 (print), 1873-6165 (electronic). URL `https://www.sciencedirect.com/science/article/pii/S1383762121001016`.

**Harris:2021:DDR**

[HH21] Sarah L. Harris and David Harris. Digital design and RISC-V computer architecture textbook. In IEEE, editor, *2021 ACM/IEEE Workshop on Computer Architecture Education (WCAE)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Harris:2022:DDC**

[HH22] Sarah Harris and David Money Harris. *Digital Design and Computer Architecture: RISC-V Edition*. Morgan Kaufmann (Elsevier), Cambridge, MA, USA, 2022. ISBN 0-12-820064-2 (paperback). xxv + 564 pp. LCCN TK7868.D5 H35 2022.

**Hubert:2023:MOO**

[HH23] Bastien Hubert and Omar Hammami. Multi-objective optimisation of RISC-V CV32A6 for ML application. In IEEE, editor, *2023 IEEE International Conference on Design, Test and Technology of Integrated Systems (DTTIS)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Holler:2019:OSR**

[HHB+19] Roland Höller, Dominic Haselberger, Dominik Ballek, Peter Rössler, Markus Krapfenbauer, and Martin Linauer. Open-source

RISC-V processor IP cores for FPGAs — overview and evaluation. In IEEE, editor, *2019 8th Mediterranean Conference on Embedded Computing (MECO)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Harmina:2023:DIC**

[HHB23] Tomislav Harmina, Daniel Hofman, and Jakov Benjak. DCT implementation on a custom FPGA RISC-V processor. In IEEE, editor, *2023 International Symposium ELMAR*, pages 163–167. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Harris:2023:CVW**

[HHTo23] Sarah Harris, David Harris, Rose Thompson, and 45 others. CORE-V Wally. Web source code archive, 2023. URL `https://github.com/openhwgroup/cvw`.

**Han:2023:RVB**

[HJ23] Shaopu Han and Yanfeng Jiang. RISC-V-based evaluation and strategy exploration of MRAM triple-level hybrid cache systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 31 (7):980–992, 2023. CODEN IEVSE9. ISSN 1063-8210 (print), 1557-9999 (electronic).

**He:2020:HPR**

[HK20] Jiongrui He and Seok-Bum Ko. High-performance RISC-V processor with improved dispatch and commit schemes. In IEEE, editor, *2020 International Conference on Electronics, Information, and Communication (ICEIC)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Heinz:2019:CHE**

[HLHK19] Carsten Heinz, Yannick Lavan, Jaco Hofmann, and Andreas Koch. A catalog and in-hardware evaluation of open-source drop-in compatible RISC-V softcore processors. In IEEE, editor, *2019 International Conference on ReConFigurable Computing and FPGAs (ReConFig)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Hammond:2024:ABC**

[HLP+24] Angus Hammond, Zongyuan Liu, Thibaut Pérami, Peter Sewell, Lars Birkedal, and Jean Pichon-Pharabod. An axiomatic basis for

computer programming on the relaxed Arm-A architecture: The AxSL logic. *Proceedings of the ACM on Programming Languages (PACMPL)*, 8 (POPL):21:1–21:??, January 2024. CODEN ???? ISSN 2475-1421 (electronic). URL `https://dl.acm.org/doi/10.1145/3632863`.

**Hussein:2021:AFG**

[HM21] Abdelrahman S. Hussein and Hassan Mostafa. ASIC-FPGA gap for a RISC-V core implementation for DNN applications. In IEEE, editor, *2021 3rd Novel Intelligent and Leading Emerging Sciences Conference (NILES)*, pages 385–388. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Hepola:2022:OCD**

[HMJ22] Kari Hepola, Joonas Multanen, and Pekka Jääskeläinen. OpenASIP 2.0: Co-design toolset for RISC-V application-specific instruction-set processors. In IEEE, editor, *2022 IEEE 33rd International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pages 161–165. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Hepola:2024:EEE**

[HMJ24] Kari Hepola, Joonas Multanen, and Pekka Jääskeläinen. Energy-efficient exposed datapath architecture with a RISC-V instruction set mode. *IEEE Transactions on Computers*, 73(2):560–573, February 2024. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Ho:2021:IDC**

[HMTL21] Van-Ninh Ho, Khai-Minh Ma, Hong-Hai Thai, and Duc-Hung Le. Implementation of a dual-core 64-bit RISC-V on 7nm FinFET process. In IEEE, editor, *2021 International Conference on Advanced Technologies for Communications (ATC)*, pages 28–32. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Horne:2020:GSF**

[Hor20] Mitchell Horne. Getting started with FreeBSD/RISC-V. *FreeBSD Journal*, ??(??):12–17, January/February 2020. URL `https://freebsdfoundation.org/wp-content/uploads/2020/03/Getting-Started-With-FreeBSD-RISC-V.pdf`.

**Horne:2021:RQ**

[Hor21a] Mitchell Horne. riscv/QEMU. Web site, June 8, 2021. URL `https://wiki.freebsd.org/riscv/QEMU`. See also [Hor20].

**Horne:2021:S**

[Hor21b] Mitchell Horne. Spike. Web site, June 8, 2021. URL `https://wiki.freebsd.org/riscv/Spike`.

**Hennessy:2018:NGA**

[HP18] John Hennessy and David Patterson. A new golden age for computer architecture: Domain-specific hardware/software co-design, enhanced. In IEEE, editor, *2018 ACM/IEEE 45th Annual International Symposium on Computer Architecture: 1–6 June 2018, Los Angeles, CA, USA*, pages 27–29. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018. ISBN 1-5386-5985-9 (e-book). LCCN QA76.9.A73 .A568 2018.

**Harris:2024:UDS**

[HSE+24] David Harris, James Stine, Milo Ercegovac, Alberto Nannarelli, Katherine Parry, and Cedar Turek. Unified digit selection for radix-4 recurrence division and square root. *IEEE Transactions on Computers*, 73(1):292–300, January 2024. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Hesham:2021:DAI**

[HSEKD21] Sarah Hesham, Mohamed Shalan, M. Watheq El-Kharashi, and Mohamed Dessouky. Digital ASIC implementation of RISC-V: OpenLane and commercial approaches in comparison. In IEEE, editor, *2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 498–502. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**He:2023:AHS**

[HSL+23] Zicheng He, Ao Sheri, Qiufeng Li, Quan Cheng, and Hao Yu. Agile hardware and software co-design for RISC-V-based multi-precision deep learning microprocessor. In IEEE, editor, *2023 28th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages 490–495. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Haribabu:2023:RVC**

[HSR+23] P Haribabu, Gvk Sasirekha, Madhav Rao, Jyotsna Bapat, and Debabrata Das.

RISC-V core for ethical intelligent IoT edge: Analysis & design choice. In IEEE, editor, *2023 IEEE/ACM 23rd International Symposium on Cluster, Cloud and Internet Computing Workshops (CCGridW)*, pages 110–117. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**He:2023:DIR**

[HSWM23] Jiangwei He, Weiwei Shi, Chaoyuan Wu, and Zhihong Mo. Design and implementation of a RISC-V SoC for real-time epilepsy detection on FPGA. In IEEE, editor, *2023 6th International Conference on Electronics Technology (ICET)*, pages 127–132. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Herdt:2021:MBC**

[HTGD21] Vladimir Herdt, Sören Tempel, Daniel Große, and Rolf Drechsler. Mutation-based compliance testing for RISC-V. In IEEE, editor, *2021 26th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages 55–60. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Hoyer:2022:DAF**

[HUL+22] Ingo Hoyer, Alexander Utz, André Lüdecke, Mike Richter, Felix Wichum, Pierre Gembaczka, Kerstin Köhler, Maurice Rohr, Christoph Hoog Antink, and Karsten Seidl. Detection of atrial fibrillation with an optimized neural network on a RISC-V-based microcontroller for efficient integration into ECG patches. In IEEE, editor, *2022 IEEE International Symposium on Medical Measurements and Applications (MeMeA)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Harris:2021:MIR**

[HVW+21] Austin Harris, Tarunesh Verma, Shijia Wei, Lauren Biernacki, Alex Kisil, Misiker Tadesse Aga, Valeria Bertacco, Baris Kasikci, Mohit Tiwari, and Todd Austin. Morpheus II: a RISC-V security extension for protecting vulnerable software and hardware. In IEEE, editor, *2021 IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, pages 226–238. IEEE Computer Society Press, 1109 Spring Street, Suite 300,

Silver Spring, MD 20910, USA, 2021.

**Hu:2022:WPR**

[HWG22] Xiao Hu, Yaohua Wang, and Xuan Gao. Work-in-progress: RISC-V based low-cost embedded trace processing system. In IEEE, editor, *2022 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pages 31–32. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Han:2023:MBC**

[HWJ23] Shaopu Han, Qiguang Wang, and Yanfeng Jiang. MRAM-based cache system design and policy optimization for RISC-V multicore CPUs. *IEEE Transactions on Magnetics*, 59 (6):1–14, 2023. CODEN IEMGAQ. ISSN 0018-9464 (print), 1941-0069 (electronic).

**Ha:2023:KCI**

[HYML23] Seon Ha, Minsang Yu, Hyungon Moon, and Jongeun Lee. Kernel code integrity protection at the physical address level on RISC-V. *IEEE Access*, 11:62358–62367, 2023. ISSN 2169-3536.

**Haj-Yahya:2019:LSB**

[HYWP+19] Jawad Haj-Yahya, Ming Ming Wong, Vikramkumar Pudi, Shivam Bhasin, and Anupam Chattopadhyay. Lightweight secure-boot architecture for RISC-V System-on-Chip. In IEEE, editor, *20th International Symposium on Quality Electronic Design (ISQED)*, pages 216–223. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**He:2022:DCG**

[HYXW22] Bin He, Ning-Mei Yu, Meng Xu, and Xing-Jia Wang. Design of computing granularity configurable processor based on RISC-V extended instruction. In IEEE, editor, *2022 IEEE 16th International Conference on Solid-State & Integrated Circuit Technology (ICSICT)*, pages 1–3. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Huang:2019:ILA**

[HZS+19] Bo-Yuan Huang, Hongce Zhang, Pramod Subramanyan, Yakir Vizel, Aarti Gupta, and Sharad Malik. Instruction-level abstraction (ILA): a uniform specification for System-on-Chip (SoC) verification. *ACM Transactions on De-*

*sign Automation of Electronic Systems*, 24(1):10:1–10:??, January 2019. CODEN ATASFO. ISSN 1084-4309 (print), 1557-7309 (electronic).

**IEEE:2021:ISC**

[IEE21] IEEE, editor. *2021 IEEE 28th Symposium on Computer Arithmetic: ARITH 2021: virtual conference, 14–16 June 2021: proceedings*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021. ISBN 1-66542-293-9 (print), 1-66544-648-X (ebook). LCCN ????

**IEEE:2022:ISC**

[IEE22] IEEE, editor. *2022 IEEE 29th Symposium on Computer Arithmetic: ARITH 2022: virtual conference, 12–14 September 2022: proceedings*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022. ISBN 1-66547-827-6, 1-66547-828-4. LCCN ????

**IEEE:2023:PIS**

[IEE23] IEEE, editor. *Proceedings: 2023 IEEE 30th Symposium on Computer Arithmetic: ARITH 2023, 4–6 September 2023 Portland, United States*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023. LCCN ????

**Ishimaru:2018:FBR**

[IFO+18] Pedro J. A. Ishimaru, Antonyus P. A. Ferreira, Vanessa O. Ogg, R. A. M. Cecil Accetti, and Edna N. S. Barros. An FPGA-Based RFID baseband processor using a RISC-V platform. In IEEE, editor, *2018 31st Symposium on Integrated Circuits and Systems Design (SBCCI)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Im:2021:CAB**

[IK21a] Jaekyung Im and Seokhyeong Kang. Comparative analysis between Verilog and Chisel in RISC-V core design and verification. In IEEE, editor, *2021 18th International SoC Design Conference (ISOCC)*, pages 59–60. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Islam:2021:ERS**

[IK21b] Md Ashraful Islam and Kenji Kise. Efficient resource shared RISC-V multicore processor. In IEEE, editor, *2021 IEEE 14th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MC-*

*SoC)*, pages 366–372. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Ince:2019:BOS**

[ILG19] M. Numan Ince, Joseph Ledet, and Melih Gunay. Building an open source Linux computing system on RISC-V. In IEEE, editor, *2019 1st International Informatics and Software Engineering Conference (UBMYK)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Imianosky:2023:IRE**

[ISM+23] Carolina Imianosky, Douglas A. Santos, Douglas R. Melo, Felipe VieE, and Luigi Dilillo. Implementation and reliability evaluation of a RISC-V vector extension unit. In IEEE, editor, *2023 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Imianosky:2020:ECC**

[IVZV20] Carolina Imianosky, Paulo R. O. Valim, Cesar A. Zeferino, and Felipe Viel. Evaluating the CCSDS 123 compressor running on RISC-V and ARM architectures. In IEEE, editor, *2020 X Brazilian Symposium on Computing Systems Engineering (SBESC)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Iuga:2022:CET**

[IZG22] Nicolai Iuga, Ionel Zagan, and Vasile Gheorghita Gaitan. CPU execution time analysis based on RISC-V ISA simulators: a survey. In IEEE, editor, *2022 International Conference on Development and Application Systems (DAS)*, pages 12–18. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Jahnke:2023:PEP**

[JBK23] Marek Jahnke, Lucas Bublitz, and Ulf Kulau. Performance evaluation of PicoRV32 RISC-V softcore for resource-constrained devices. In IEEE, editor, *2023 IEEE Nordic Circuits and Systems Conference (NorCAS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Jang:2021:DMP**

[JHL+21] Hyeonguk Jang, Kyuseung Han, Sukho Lee, Jae-Jin Lee, Seung-Yeong Lee, Jae-Hyoung Lee, and Woo-joo Lee. Developing a multicore platform utilizing open RISC-V cores. *IEEE Access*, 9:120010–120023, 2021. ISSN 2169-3536.

**Jiao:2021:RVR**

[JHLD21] Qiang Jiao, Wei Hu, Fang Liu, and Yong Dong. RISC-VTF: RISC-V based extended instruction set for Transformer. In IEEE, editor, *2021 IEEE International Conference on Systems, Man, and Cybernetics (SMC)*, pages 1565–1570. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Jin:2023:SBS**

[JHQ23] Hai Jin, Zhuo He, and Weizhong Qiang. SpecTerminator: Blocking speculative side channels based on instruction classes on RISC-V. *ACM Transactions on Architecture and Code Optimization*, 20(1):15:1–15:??, March 2023. CODEN ???? ISSN 1544-3566 (print), 1544-3973 (electronic). URL `https://dl.acm.org/doi/10.1145/3566053`.

**Johns:2020:MRV**

[JK20] Matthew Johns and Tom J. Kazmierski. A minimal RISC-V vector processor for embedded systems. In IEEE, editor, *2020 Forum for Specification and Design Languages (FDL)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Jimenez:2023:FVR**

[JRD+23] Victor Jimenez, Mario Rodriguez, Marc Dominguez, Josep Sans, Ivan Diaz, Luca Valente, Vito Luca Guglielmi, Josue V. Quiroga, R. Ignacio Genovese, Nehir Sonmez, Oscar Palomar, and Miquel Moreto. Functional verification of a RISC-V vector accelerator. *IEEE Design & Test*, 40(3):36–44, 2023. ISSN 2168-2356 (print), 2168-2364 (electronic).

**Joannou:2023:RTR**

[JRW+23] Alexandre Joannou, Peter Rugg, Jonathan Woodruff, Franz A. Fuchs, Marno Van der Maas, Matthew Naylor, Michael Roe, Robert N. M. Watson, Peter G. Neumann, and Simon W. Moore. Randomized testing of RISC-V CPUs using direct instruction injection. *IEEE Design & Test*, page 1, 2023. ISSN 2168-2356 (print), 2168-2364 (electronic).

**Jose:2023:SME**

[JS23] Tom Jose and Deepak Shankar. System model evaluation of RISC-V cores for improved performance and fault tolerance. In IEEE, editor, *2023 IEEE Space Computing Conference (SCC)*, pages 86–91. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Jain:2020:IEB**

[JSB20] Vineet Jain, Abhishek Sharma, and Eduardo Augusto Bezerra. Implementation and extension of bit manipulation instruction on RISC-V architecture using FPGA. In IEEE, editor, *2020 IEEE 9th International Conference on Communication Systems and Network Technologies (CSNT)*, pages 167–172. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Jiang:2023:FAU**

[JZWL23] Shijie Jiang, Yi Zou, Hao Wang, and Wanwan Li. An FFT accelerator using deeply-coupled RISC-V instruction set extension for arbitrary number of points. In IEEE, editor, *2023 IEEE 34th International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pages 165–171. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Karabulut:2020:RRV**

[KA20] Emre Karabulut and Aydin Aysu. RANTT: a RISC-V architecture extension for the number theoretic transform. In IEEE, editor, *2020 30th International Conference on Field-Programmable Logic and Applications (FPL)*, pages 26–32. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Koppelmann:2019:RVE**

[KAMS19] Bastian Koppelmann, Peer Adelt, Wolfgang Mueller, and Christoph Scheytt. RISC-V extensions for bit manipulation instructions. In IEEE, editor, *2019 29th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, pages 41–48. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Kamaleldin:2019:MMS**

[KAR+19] Ahmed Kamaleldin, Muhammad Ali, Pedram Amini Rad, Marcus Gottschalk,

and Diana Göhringer. Modular memory system for RISC-V based MPSoCs on Xilinx FPGAs. In IEEE, editor, *2019 IEEE 13th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MC-SoC)*, pages 68–73. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Koenig:2017:HAC**

[KBBA17] Jack Koenig, David Biancolin, Jonathan Bachrach, and Krste Asanovic. A hardware accelerator for computing an exact dot product. In Burgess et al. [BBdD17], pages 114–121. ISBN 1-5386-1966-0 (print), 1-5386-1965-2, 1-5386-1964-4. ISSN 1063-6889. LCCN QA76.9.C62 S95 2017. URL `http://ieeexplore.ieee.org/servlet/opac?punumber=8019911`.

**Kressel:2023:EIO**

[KCGL23] John Alistair Kressel, Guillermo Callaghan, Cosmin Gorgovan, and Mikel Luján. Evaluating the impact of optimizations for dynamic binary modification on 64-bit RISC-V. In IEEE, editor, *2023 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pages 81–91. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Kumar:2019:ISR**

[KCHYM19] Vinay B. Y. Kumar, Anupam Chattopadhyay, Jawad Haj-Yahya, and Avi Mendelson. ITUS: a secure RISC-V System-on-Chip. In IEEE, editor, *2019 32nd IEEE International System-on-Chip Conference (SOCC)*, pages 418–423. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Keller:2017:RVP**

[KCZ+17] Ben Keller, Martin Cochet, Brian Zimmer, Jaehwa Kwak, Alberto Puggelli, Yunsup Lee, Milovan Blagojević, Stevo Bailey, Pi-Feng Chiu, Palmer Dabbelt, Colin Schmidt, Elad Alon, Krste Asanović, and Borivoje Nikolić. A RISC-V processor SoC with integrated power management at sub-microsecond timescales in 28 nm FD-SOI. *IEEE Journal of Solid-State Circuits*, 52(7):1863–1875, 2017. CODEN IJSCBC. ISSN 0018-9200 (print), 1558-173X (electronic).

**Khamis:2018:CRV**

[KEAS+18] Mostafa Khamis, Sameh El-Ashry, Ahmed Shalaby, Mohamed AbdElsalam, and

M. Watheq El-Kharashi. A configurable RISC-V for NoC-based MPSoCs: a framework for hardware emulation. In IEEE, editor, *2018 11th International Workshop on Network on Chip Architectures (NoCArc)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Kuo:2023:IRT**

[KFGH+23] Yao-Ming Kuo, Mark F. Flanagan, Francisco Garcia-Herrero, Óscar Ruano, and Juan Antonio Maestro. Integration of a real-time CCSDS 410.0-B-32 error-correction decoder on FPGA-Based RISC-V SoCs using RISC-V vector extension. *IEEE Transactions on Aerospace and Electronic Systems*, 59(5): 5835–5846, 2023. CODEN IEARAX. ISSN 0018-9251 (print), 1557-9603 (electronic).

**Kanamoto:2019:SSR**

[KFK+19] Toshiki Kanamoto, Masami Fukushima, Koichi Kitagishi, Seijin Nakayama, Hideki Ishihara, Koki Kasai, Atsushi Kurokawa, and Masashi Imai. A single-stage RISC-V processor to mitigate the von Neumann bottleneck. In IEEE, editor, *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 1085–1088. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Karl:2022:HAF**

[KFS22] Patrick Karl, Tim Fritzmann, and Georg Sigl. Hardware accelerated FrodoKEM on RISC-V. In IEEE, editor, *2022 25th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, pages 154–159. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Kapre:2017:HDR**

[KG17] Nachiket Kapre and Jan Gray. Hoplite: a deflection-routed directional torus NoC for FPGAs. *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 10(2):14:1–14:??, April 2017. CODEN ???? ISSN 1936-7406 (print), 1936-7414 (electronic).

**Kamaleldin:2022:AAH**

[KG22a] Ahmed Kamaleldin and Diana Göhringer. AGILER: an adaptive heterogeneous tile-based many-core architecture for RISC-V proces-

sors. *IEEE Access*, 10: 43895–43913, 2022. ISSN 2169-3536.

**Kamaleldin:2022:HMA**

[KG22b] Ahmed Kamaleldin and Diana Göhringer. A hybrid memory/accelerator tile architecture for FPGA-based RISC-V manycore systems. In IEEE, editor, *2022 32nd International Conference on Field-Programmable Logic and Applications (FPL)*, pages 300–306. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Klemmer:2022:EPM**

[KG22c] Lucas Klemmer and Daniel Große. An exploration platform for microcoded RISC-V cores leveraging the one instruction set computer principle. In IEEE, editor, *2022 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pages 38–43. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Koranek:2022:IRO**

[KGBH22] Daniel F. Koranek, Scott R. Graham, Brett J. Borghetti, and Wayne C. Henry. Identification of return-oriented programming attacks using RISC-V instruction trace data. *IEEE Access*, 10: 45347–45364, 2022. ISSN 2169-3536.

**Keilbart:2024:DIC**

[KGC+24] Chris Keilbart, Yuhui Gao, Martin Chua, Eric Matthews, Steven J. E. Wilton, and Lesley Shannon. Designing an IEEE-compliant FPU that supports configurable precision for soft processors. *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 17(2): 33:1–33:??, June 2024. CODEN ???? ISSN 1936-7406 (print), 1936-7414 (electronic). URL `https://dl.acm.org/doi/10.1145/3650036`.

**Kuo:2023:RVG**

[KGHRM23] Yao-Ming Kuo, Francisco García-Herrero, Oscar Ruano, and Juan Antonio Maestro. RISC-V Galois Field ISA extension for non-binary error-correction codes and classical and post-quantum cryptography. *IEEE Transactions on Computers*, 72(3):682–692, March 2023. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Kamaleldin:2020:TMR**

[KHG20] Ahmed Kamaleldin, Salma Hesham, and Diana Göhringer. Towards a modular RISC-V based many-core architecture for FPGA accelerators. *IEEE Access*, 8:

148812–148826, 2020. ISSN 2169-3536.

**Kong:2022:HPR**

[KHH22] Xinjie Kong, Weiliang He, and Jun Han. A high-performance RISC-V co-processor architecture for fast IP processing. In IEEE, editor, *2022 IEEE 16th International Conference on Solid-State & Integrated Circuit Technology (ICSICT)*, pages 1–3. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Korsman:2023:EEM**

[KHS+23] Aleksi Korsman, Verneri Hirvonen, Otto Simola, Antti Tarkka, Marko Kosunen, and Jussi Ryynänen. End-to-end multi-target verification environment for a RISC-V microprocessor. In IEEE, editor, *2023 19th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Kadomoto:2020:RVP**

[KIS20] Junichiro Kadomoto, Hidetsugu Irie, and Shuichi Sakai. A RISC-V processor with an inter-chiplet wireless communication interface for shape-changeable computers. In IEEE, editor, *2020 IEEE Symposium in Low-Power and High-Speed Chips (COOL CHIPS)*, pages 1–3. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Kadomoto:2022:EDM**

[KIS22] Junichiro Kadomoto, Hidetsugu Irie, and Shuichi Sakai. Evaluation of different microarchitectures for energy-efficient RISC-V cores. In IEEE, editor, *2022 IEEE 15th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC)*, pages 78–84. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Kanamori:2021:ROR**

[KK21] Takuto Kanamori and Kenji Kise. RVCoreP-32IC: an optimized RISC-V soft processor supporting the compressed instructions. In IEEE, editor, *2021 IEEE 14th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC)*, pages 38–45. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver

Spring, MD 20910, USA, 2021.

**Kurian:2023:PER**

[KK23] Ashley Kurian and M. Ramesh Kini. Posit extended RISC-V processor and its enhancement using data type casting. In *Lecture Notes in Networks and Systems*, pages 571–586. Springer Nature, Singapore, 2023. ISBN 981-19663-4-6. ISSN 2367-3389.

**Kim:2016:SCD**

[KKC+16] Channoh Kim, Sungmin Kim, Hyeon Gyu Cho, Dooyoung Kim, Jaehyeok Kim, Young H. Oh, Hakbeom Jang, and Jae W. Lee. Short-circuit dispatch: accelerating virtual machine interpreters on embedded processors. *ACM SIGARCH Computer Architecture News*, 44(3):291–303, June 2016. CODEN CANED2. ISSN 0163-5964 (print), 1943-5851 (electronic).

**Kwon:2022:OIS**

[KKE+22] Hyeokdong Kwon, Hyunjun Kim, Siwoo Eum, Minjoo Sim, Hyunji Kim, Wai-Kong Lee, Zhi Hu, and Hwajeong Seo. Optimized implementation of SM4 on AVR microcontrollers, RISC-V processors, and ARM processors. *IEEE Access*, 10:80225–80233, 2022. ISSN 2169-3536.

**Kukner:2022:RVP**

[KKEG22] Halil Kükner, Gökhan Kaplayan, Ahmet Efe, and Mehmet Ali Gülden. RISC-V processor trace encoder with multiple instructions retirement support. In IEEE, editor, *2022 IFIP/IEEE 30th International Conference on Very Large Scale Integration (VLSI-SoC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Kim:2020:FCC**

[KKH+20] Jungwoo Kim, Jae Min Kim, Sangwook Han, Pritesh Vora, Pranav Dayal, Hyunggi Kim, Jonghwan Lee, Daeyoung Yoon, Jeiyoung Lee, Tienyu Chang, Ivan Siu-Chuang Lu, Kee-Bong Song, Sang Won Son, and Jongwoo Lee. A flexible control and calibration architecture using RISC-V MCU for 5G millimeter-wave mobile RF transceivers. In IEEE, editor, *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 203–206. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Kim:2017:TAAa**

[KKK+17a] Channoh Kim, Jaehyeok

Kim, Sungmin Kim, Dooyoung Kim, Namho Kim, Gitae Na, Young H. Oh, Hyeon Gyu Cho, and Jae W. Lee. Typed architectures: Architectural support for lightweight scripting. *ACM SIGARCH Computer Architecture News*, 45(1):77–90, March 2017. CODEN CANED2. ISSN 0163-5964 (print), 1943-5851 (electronic).

**Kim:2017:TAAb**

[KKK+17b] Channoh Kim, Jaehyeok Kim, Sungmin Kim, Dooyoung Kim, Namho Kim, Gitae Na, Young H. Oh, Hyeon Gyu Cho, and Jae W. Lee. Typed architectures: Architectural support for lightweight scripting. *Operating Systems Review*, 51(2):77–90, June 2017. CODEN OSRED8. ISSN 0163-5980 (print), 1943-586X (electronic).

**Kim:2017:TAAc**

[KKK+17c] Channoh Kim, Jaehyeok Kim, Sungmin Kim, Dooyoung Kim, Namho Kim, Gitae Na, Young H. Oh, Hyeon Gyu Cho, and Jae W. Lee. Typed architectures: Architectural support for lightweight scripting. *ACM SIGPLAN Notices*, 52(4):77–90, April 2017. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

**Kimura:2019:PSV**

[KKOY19] Yoshiki Kimura, Tomoya Kikuchi, Kanemitsu Ootsu, and Takashi Yokota. Proposal of scalable vector extension for embedded RISC-V soft-core processor. In IEEE, editor, *2019 Seventh International Symposium on Computing and Networking Workshops (CANDARW)*, pages 435–439. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Kim:2020:RIL**

[KLP+20] Haeyoung Kim, Jinjae Lee, Derry Pratama, Asep Muhamad Awaludin, Howon Kim, and Donghyun Kwon. RIMI: Instruction-level memory isolation for embedded systems on RISC-V. In IEEE, editor, *2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, pages 1–9. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Kanase:2021:ADB**

[KM21] Gopal Kanase and Nithin M. ASIC design of a 32-bit low power RISC-V based system core for medical applications. In IEEE,

editor, *2021 6th International Conference on Communication and Electronics Systems (ICCES)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Kuhne:2022:POF**

[KMB22] Jonas Kühne, Michele Magno, and Luca Benini. Parallelizing optical flow estimation on an ultra-low power RISC-V cluster for Nano-UAV navigation. In IEEE, editor, *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 301–305. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Kovacevic:2022:RVV**

[KMS22] Nikola Kovačević, Đorde Mišeljić, and Aleksa Stojković. RISC-V vector processor for acceleration of machine learning algorithms. In IEEE, editor, *2022 30th Telecommunications Forum (TELFOR)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Kazemi:2021:DVA**

[KNK+21] Zahra Kazemi, Amin Norollah, Afef Kchaou, Mahdi Fazeli, David Hely, and Vincent Beroulle. An in-depth vulnerability analysis of RISC-V micro-architecture against fault injection attack. In IEEE, editor, *2021 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**K:2024:FFA**

[KR24] Keerthi K and Chester Rebeiro. FortiFix: a fault attack aware compiler framework for crypto implementations. *ACM Transactions on Design Automation of Electronic Systems*, 29(5): 92:1–92:??, September 2024. CODEN ATASFO. ISSN 1084-4309 (print), 1557-7309 (electronic). URL `https://dl.acm.org/doi/10.1145/3650029`.

**Knodtel:2022:SID**

[KRR22] Johannes Knödtel, Sebastian Rachuj, and Marc Reichenbach. Suitability of ISAs for data paths based on redundant number systems: Is RISC-V the best? In IEEE, editor, *2022 25th Euromicro Conference on Digital System Design (DSD)*, pages 247–253. IEEE Computer Society Press, 1109 Spring

Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Kim:2022:OIP**

[KS22] Youngbeom Kim and Seog Chung Seo. Optimized implementation of PIPO block cipher on 32-bit ARM and RISC-V processors. *IEEE Access*, 10:97298–97309, 2022. ISSN 2169-3536.

**K:2021:CAD**

[KSAL21] Shalini K, Abhishek Kumar Srivastava, Surendra Allam, and Dilip Lilaramani. Comparative analysis on deep convolution neural network models using Pytorch and OpenCV DNN frameworks for identifying optimum fruit detection solution on RISC-V architecture. In IEEE, editor, *2021 IEEE Mysore Sub Section International Conference (MysuruCon)*, pages 738–743. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Karl:2024:PQS**

[KSFS24] Patrick Karl, Jonas Schupp, Tim Fritzmann, and Georg Sigl. Post-quantum signatures on RISC-V with hardware acceleration. *ACM Transactions on Embedded Computing Systems*, 23(2): 30:1–30:??, March 2024. CODEN ???? ISSN 1539-9087 (print), 1558-3465 (electronic). URL `https://dl.acm.org/doi/10.1145/3579092`.

**Kra:2023:HLP**

[KSRT23] Yehuda Kra, Yonatan Shoshan, Yehuda Rudin, and Adam Teman. HAMSA-DI: a low-power dual-issue RISC-V core targeting energy-efficient embedded systems. *IEEE Transactions on Circuits and Systems I: Regular Papers*, pages 1–14, 2023. ISSN 1549-8328 (print), 1558-0806 (electronic).

**Karmakar:2023:HSI**

[KSSMRB23] Apurba Karmakar, Santiago Sánchez-Solano, Macarena C. Martínez-Rodríguez, and Piedad Brox. HW/SW implementation of RSA digital signature on a RISC-V-based System-on-Chip. In IEEE, editor, *2023 38th Conference on Design of Circuits and Integrated Systems (DCIS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Koca:2021:MLP**

[KYDÖ21] Nazim Altar Koca, Berkay Yildiz, Yusuf Caner Demirkol, and Berna Örs. Multi-layer perceptron hardware accelerator on RISC-V processor. In IEEE, editor, *2021 13th*

*International Conference on Electrical and Electronics Engineering (ELECO)*, pages 465–469. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Kuang:2022:HSN**

[KZH22] Honglin Kuang, Yifan Zhao, and Jun Han. A high-speed NTT-based polynomial multiplication accelerator with vector extension of RISC-V for Saber algorithm. In IEEE, editor, *2022 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pages 592–595. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Laurent:2019:FIH**

[LBDPP19] Johan Laurent, Vincent Beroulle, Christophe Deleuze, and Florian Pebay-Peyroula. Fault injection on hidden registers in a RISC-V Rocket processor and software countermeasures. In IEEE, editor, *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 252–255. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Lai:2021:IBR**

[LCCS21] Jin-Yang Lai, Chiung-An Chen, Shih-Lun Chen, and Chun-Yu Su. Implement 32-bit RISC-V architecture processor using Verilog HDL. In IEEE, editor, *2021 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS)*, pages 1–2. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Li:2023:EAA**

[LCF23] Jia-Yu Li, Yi-Kai Chen, and Wai-Chi Fang. An edge AI accelerator design based on LRCN model for real-time EEG-based emotion detection system on the RISC-V FPGA platform. In IEEE, editor, *2023 IEEE 12th Global Conference on Consumer Electronics (GCCE)*, pages 89–90. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Li:2023:CCC**

[LCG+23] Ang Li, Ting-Jung Chang, Fei Gao, Tuan Ta, Georgios Tziantzioulis, Yanghui Ou, Moyang Wang, Jinzheng Tu, Kaifeng Xu, Paul Jackson, August Ning, Grigory Chirkov, Marcelo Orenes-Vera, Shady Agwa, Xiaoyu

Yan, Eric Tang, Jonathan Balkind, Christopher Batten, and David Wentzlaff. CIFER: a cache-coherent 12-nm 16-mm2 SoC with four 64-bit RISC-V application cores, 18 32-bit RISC-V compute cores, and a 1541 LUT6/mm2 synthesizable eFPGA. *IEEE Solid-State Circuits Letters*, 6: 229–232, 2023. ISSN 2573-9603.

**Lee:2023:DDB**

[LCN+23] Seunghyun Lee, Jeik Choi, Seockhwan Noh, Jahyun Koo, and Jaeha Kung. DBPS: Dynamic block size and precision scaling for efficient DNN training supported by RISC-V ISA extensions. In IEEE, editor, *2023 60th ACM/IEEE Design Automation Conference (DAC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Li:2024:TLV**

[LCW+24] Tianzheng Li, Enfang Cui, Yuting Wu, Qian Wei, and Yue Gao. TeleVM: a lightweight virtual machine for RISC-V architecture. *IEEE Computer Architecture Letters*, 23(1):121–124, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).

**Lee:2020:RVF**

[LCYK20] Jaewon Lee, Hanning Chen, Jeffrey Young, and Hyesoon Kim. RISC-V FPGA platform toward ROS-based robotics application. In IEEE, editor, *2020 30th International Conference on Field-Programmable Logic and Applications (FPL)*, page 370. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Ledin:2022:MCA**

[LF22] Jim Ledin and Dave Farley. *Modern Computer Architecture and Organization: Learn x86, ARM, and RISC-V architectures and the design of smartphones, PCs, and cloud servers*. Packt Publishing, Birmingham, UK, second edition, 2022. ISBN 1-80323-451-2 (paperback), 1-80323-823-2 (e-book). xxxvi + 628 pp. LCCN QA76.9.A73 L43 2022.

**Li:2017:ADS**

[LGB17] Lei Li, Michael Gautschi, and Luca Benini. Approximate DIV and SQRT instructions for the RISC-V ISA: an efficiency vs. accuracy analysis. In IEEE, editor, *2017 27th International Symposium on Power and Timing Modeling, Optimization and Sim-*

*ulation (PATMOS)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017.

**Li:2019:DIC**

[LHC19] Zhenhao Li, Wei Hu, and Shuang Chen. Design and implementation of CNN custom processor based on RISC-V architecture. In IEEE, editor, *2019 IEEE 21st International Conference on High Performance Computing and Communications; IEEE 17th International Conference on Smart City; IEEE 5th International Conference on Data Science and Systems (HPCC/SmartCity/DSS)*, pages 1945–1950. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Lee:2021:RVC**

[LHC+21] Shuenn-Yuh Lee, Yi-Wen Hung, Yao-Tse Chang, Chou-Ching Lin, and Gia-Shing Shieh. RISC-V CNN coprocessor for real-time epilepsy detection in wearable application. *IEEE Transactions on Biomedical Circuits and Systems*, 15(4):679–691, 2021. ISSN 1932-4545 (print), 1940-9990 (electronic).

**Le:2021:RTC**

[LHD+21] Anh-Tien Le, Trong-Thuc Hoang, Ba-Anh Dao, Akira Tsukamoto, Kuniyasu Suzaki, and Cong-Kha Pham. A real-time cache side-channel attack detection system on RISC-V out-of-order processor. *IEEE Access*, 9: 164597–164612, 2021. ISSN 2169-3536.

**Le:2022:SAD**

[LHD+22] Anh-Tien Le, Trong-Thuc Hoang, Ba-Anh Dao, Akira Tsukamoto, Kuniyasu Suzaki, and Cong-Kha Pham. Spectre attack detection with neutral network on RISC-V processor. In IEEE, editor, *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 2467–2471. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Liu:2023:BPA**

[LHK23] Yen-Fu Liu, Chou-Ying Hsieh, and Sy-Yen Kuo. Boomerang: Physical-aware design space exploration framework on RISC-V SonicBOOM microarchitecture. In IEEE, editor, *2023 IEEE 34th International Conference on Application-specific Systems, Architectures and Processors (ASAP): ASAP 2023, 19–21 July 2023, Porto, Portugal*, pages 85–

93. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, July 2023.

**Li:2021:LPA**

[LHT+21] Zhiyu Li, Yuhao Huang, Longfeng Tian, Ruimin Zhu, Shanlin Xiao, and Zhiyi Yu. A low-power asynchronous RISC-V processor with propagated timing constraints method. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 68(9):3153–3157, 2021. ISSN 1549-7747 (print), 1558-3791 (electronic).

**Liu:2021:WPR**

[Liu21] Meng Liu. Work-in-progress: The RISC-V instruction set architecture optimization and fixed-point math library co-design. In IEEE, editor, *2021 International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, pages 23–24. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Lee:2023:SDD**

[LKHK23] Jimin Lee, Jae Min Kim, Junho Huh, and Jungwoo Kim. Software-driven debug framework for embedded RISC-V, that transparently emulates the industry standard debug framework. In IEEE, editor, *2023 IEEE International Conference on Consumer Electronics (ICCE)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Lee:2022:PQC**

[LKKK22] Jihye Lee, Whijin Kim, Sohyeon Kim, and Ji-Hoon Kim. Post-quantum cryptography coprocessor for RISC-V CPU core. In IEEE, editor, *2022 International Conference on Electronics, Information, and Communication (ICEIC)*, pages 1–2. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Lu:2021:DAI**

[LLL+21] Yuan Lu, Yangmeng Liu, Yongbo Liao, Yuting Liu, and Lu Xu. Design of adjacent interconnect processor based on RISC-V. In IEEE, editor, *2021 IEEE 4th International Conference on Electronics Technology (ICET)*, pages 427–431. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Loh:2022:VDC**

[LLS22] Siu Hong Loh, You Hong Liew, and Jia Jia Sim. VLSI design course with verification of RISC-V design using universal verification methodology (UVM). In IEEE, editor, *2022 IEEE 12th International Conference on Control System, Computing and Engineering (ICCSCE)*, pages 7–12. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Li:2023:MPC**

[LMP23] Huimin Li, Nele Mentens, and Stjepan Picek. Maximizing the potential of custom RISC-V vector extensions for speeding up SHA-3 hash functions. In IEEE, editor, *2023 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Ling:2021:OSF**

[LNA21] Xiaoyi Ling, Takahiro Notsu, and Jason Anderson. An open-source framework for the generation of RISC-V processor + CGRA accelerator systems. In IEEE, editor, *2021 24th Euromicro Conference on Digital System Design (DSD)*, pages 35–42. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Luchterhandt:2023:TRC**

[LNB+23] Lars Luchterhandt, Tom Nellius, Robert Beck, Rainer Doemer, Pascal Kneuper, Wolfgang Mueller, and Babak Sadiye. Towards a Rocket Chip based implementation of the RISC-V GPC architecture. In IEEE, editor, *MBMV 2023; 26th Workshop*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Lodea:2022:ESE**

[LNZ+22] Nicolas Lodéa, Willian Nunes, Vitor Zanini, Marcos Sartori, Luciano Ost, Ney Calazans, Rafael Garibotti, and César Marcon. Early soft error reliability analysis on RISC-V. *IEEE Latin America Transactions*, 20(9):2139–2145, 2022. ISSN 1548-0992.

**Lee:2021:MCS**

[LPB+21] Wooyoung Lee, Jina Park, Changjun Byun, Eunjin Choi, Jae-Hyoung Lee, Woojoo Lee, Kyung Jin Byun, and Kyuseung Han. $K$-means clustering-specific lightweight RISC-V processor. In IEEE, editor, *2021*

*18th International SoC Design Conference (ISOCC)*, pages 391–392. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Liu:2022:RVS**

[LPL22] Youyao Liu, Yuchen Pan, and Longyi Li. Research on vector structure of neural network algorithm based on RISC-V. In IEEE, editor, *2022 14th International Conference on Measuring Technology and Mechatronics Automation (ICMTMA)*, pages 134–139. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Liu:2019:RGH**

[LPZ19] Gai Liu, Joseph Primmer, and Zhiru Zhang. Rapid generation of high-quality RISC-V processors from functional instruction set specifications. In IEEE, editor, *2019 56th ACM/IEEE Design Automation Conference (DAC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Lupori:2018:THP**

[LRB18] Leandro Lupori, Vanderson Rosario, and Edson Borin. Towards a high-performance RISC-V emulator. In IEEE, editor, *2018 Symposium on High Performance Computing Systems (WSCAD)*, pages 213–220. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Lamberti:2021:LPL**

[LRF+21] Lorenzo Lamberti, Manuele Rusci, Marco Fariselli, Francesco Paci, and Luca Benini. Low-power license plate detection and recognition on a RISC-V multicore MCU-based vision system. In IEEE, editor, *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Leplus:2022:IRD**

[LSB22] Gaëtan Leplus, Olivier Savry, and Lilian Bossuet. Insertion of random delay with context-aware dummy instructions generator in a RISC-V processor. In IEEE, editor, *2022 IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, pages 81–84. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Lu:2021:SRV**

[Lu21a] T. Lu. A survey on RISC-V security: Hardware and architecture. *arXiv.org*, ??(??):30, July 9, 2021. URL `https://arxiv.org/abs/2107.04175`.

**Lu:2021:ESD**

[Lu21b] Tao Lu. Exploring storage device characteristics of a RISC-V little-core SoC. In IEEE, editor, *2021 IEEE International Conference on Networking, Architecture and Storage (NAS)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Lu:2022:DPP**

[Lu22] Liu Lu. Design of a programmable PCI-E encryption system based on RISC-V. In IEEE, editor, *2022 6th International Symposium on Computer Science and Intelligent Control (ISCSIC)*, pages 368–373. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Lopez-Villellas:2023:RVG**

[LVPSB+23] Lorién López-Villellas, Esteve Pineda-Sánchez, Asaf Badouh, Santiago Marco-Sola, Pablo Ibáñez, Jesús Alastruey-Benedé, and Miquel Moretó. RISC-V for genome data analysis: Opportunities and challenges. In IEEE, editor, *2023 38th Conference on Design of Circuits and Integrated Systems (DCIS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Lima:2020:ORV**

[LVR+20] Pedro Lima, Caio Vieira, Jorge Reis, Alexandre Almeida, Jarbas Silveira, Roger Goerl, and César Marcon. Optimizing RISC-V ISA usage by sharing coprocessors on MPSoC. In IEEE, editor, *2020 IEEE Latin-American Test Symposium (LATS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Lee:2014:DPG**

[LWA+14] Yunsup Lee, Andrew Waterman, Rimas Avizienis, Henry Cook, Chen Sun, Vladimir Stojanović, and Krste Asanović. A 45nm 1.3GHz 16.7 double-precision GFLOPS/W RISC-V processor with vector accelerators. In IEEE, editor, *ESSCIRC 2014 — 40th European Solid State Circuits Conference (ESSCIRC)*, pages 199–202. IEEE Computer Society

Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2014.

**Lee:2016:AAB**

[LWC+16] Yunsup Lee, Andrew Waterman, Henry Cook, Brian Zimmer, Ben Keller, Alberto Puggelli, Jaehwa Kwak, Ruzica Jevtic, Stevo Bailey, Milovan Blagojevic, Pi-Feng Chiu, Rimas Avizienis, Brian Richards, Jonathan Bachrach, David Patterson, Elad Alon, Bora Nikolic, and Krste Asanovic. An agile approach to building RISC-V microprocessors. *IEEE Micro*, 36(2):8–20, March/April 2016. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic). URL `http://www.computer.org/csdl/mags/mi/2016/02/mmi2016020008-abs.html`.

**Leidel:2018:GRV**

[LWC18] John D. Leidel, Xi Wang, and Yong Chen. GoblinCore-64: a RISC-V based architecture for data intensive computing. In IEEE, editor, *2018 IEEE High Performance extreme Computing Conference (HPEC)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Li:2020:IMS**

[LWD20] Renwei Li, Junning Wu, and Enqiang Dai. An improved M/T speed algorithm based on RISC-V DSP. In IEEE, editor, *2020 International Conference on Intelligent Computing, Automation and Systems (ICICAS)*, pages 105–108. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Li:2023:SCE**

[LWLA23] Wenxin Li, Weike Wang, Senyang Li, and Zhenliang An. A static CFG extraction scheme for RISC-V runtime CFI. In IEEE, editor, *2023 9th International Symposium on System Security, Safety, and Reliability (ISSSR)*, pages 444–445. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Liang:2023:IHI**

[LXC23] Quanyi Liang, Shaobin Xie, and Boyang Cai. Intelligent home IoT intrusion detection system based on RISC-V. In IEEE, editor, *2023 IEEE 3rd International Conference on Power, Electronics and Computer Applications (ICPECA)*, pages 296–300. IEEE Computer

Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Li:2023:PDC**

[LYL23] Kai Li, Wei Yin, and Qiang Liu. A portable DSP coprocessor design using RISC-V packed-SIMD instructions. In IEEE, editor, *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Lei:2020:HRP**

[LYZH20] Mai Lei, Tian-Yu Yin, Yu-Chao Zhou, and Jun Han. Highly reconfigurable performance monitoring unit on RISC-V. In IEEE, editor, *2020 IEEE 15th International Conference on Solid-State & Integrated Circuit Technology (ICSICT)*, pages 1–3. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Lu:2020:DIS**

[LZH20] Liangliang Lu, Ming Zhang, and Dingxin He. Design and implementation of a smart home system based on the RISC-V processor. In IEEE, editor, *2020 IEEE 2nd International Conference on Civil Aviation Safety and Information Technology (ICCASIT)*, pages 300–304. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Lee:2015:RRV**

[LZW+15] Yunsup Lee, Brian Zimmer, Andrew Waterman, Alberto Puggelli, Jaehwa Kwak, Ruzica Jevtic, Ben Keller, Stevo Bailey, Milovan Blagojevic, Pi-Feng Chiu, Henry Cook, Rimas Avizienis, Brian Richards, Elad Alon, Borivoje Nikolic, and Krste Asanovic. Raven: a 28nm RISC-V vector processor with integrated switched-capacitor DC-DC converters and adaptive clocking. In IEEE, editor, *2015 IEEE Hot Chips 27 Symposium (HCS)*, pages 1–45. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2015.

**Matthews:2018:EPE**

[MAS18] Eric Matthews, Zavier Aguila, and Lesley Shannon. Evaluating the performance efficiency of a soft-processor, variable-length, parallel-execution-unit architecture for FPGAs using the RISC-V ISA. In IEEE, editor, *2018 IEEE 26th Annual International Symposium on*

*Field-Programmable Custom Computing Machines (FCCM)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Melo:2016:OBP**

[MB16] Cecil Accetti R. A. Melo and Edna Barros. Oolong: a baseband processor extension to the RISC-V ISA. In IEEE, editor, *2016 IEEE 27th International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pages 241–242. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2016.

**Maisto:2022:PVU**

[MC22] Vincenzo Maisto and Alessandro Cilardo. A pluggable vector unit for RISC-V vector extension. In IEEE, editor, *2022 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1143–1148. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Mumcu:2022:PEL**

[MÇB22] Muhammet Cihat Mumcu, İhsan Çiçek, and Salih Bayar. Performance evaluation of lightweight cryptographic algorithms on RISC-V. In IEEE, editor, *2022 30th Signal Processing and Communications Applications Conference (SIU)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Ma:2021:CRV**

[MCL+21] Jun Ma, Ting Chong, Lei Li, Hao Liu, Xige Zhang, Liang Liu, and Yidong Yuan. Construction of RISC-V lightweight trusted execution environment based on hardware extension. In IEEE, editor, *2021 IEEE International Conference on Power, Intelligent Computing and Systems (ICPICS)*, pages 237–242. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Ma:2022:DSB**

[MCL22] Khai-Minh Ma, Tran-Bao-Thuong Cao, and Duc-Hung Le. Design of an SoC based on 32-bit RISC-V CPU and lightweight block cipher PRINCE on FPGA. In IEEE, editor, *2022 9th NAFOSTED Conference on Information and Computer Science (NICS)*, pages 25–29. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Mallasen:2024:BPE**

[MDPM24] David Mallasén, Alberto A. Del Barrio, and Manuel Prieto-Matias. Big-PERCIVAL: Exploring the native use of 64-bit posit arithmetic in scientific computing. *IEEE Transactions on Computers*, 73(6):1472–1485, June 2024. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Morales:2019:LAD**

[MDR19] Hanssel Morales, Ckristian Duran, and Elkim Roa. A low-area direct memory access controller architecture for a RISC-V based low-power microcontroller. In IEEE, editor, *2019 IEEE 10th Latin American Symposium on Circuits & Systems (LASCAS)*, pages 97–100. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Mashimo:2019:OSF**

[MFM+19] Susumu Mashimo, Akifumi Fujita, Reoma Matsuo, Seiya Akaki, Akifumi Fukuda, Toru Koizumi, Junichiro Kadomoto, Hidetsugu Irie, Masahiro Goshima, Koji Inoue, and Ryota Shioya. An open source FPGA-Optimized out-of-order RISC-V soft processor. In IEEE, editor, *2019 International Conference on Field-Programmable Technology (ICFPT)*, pages 63–71. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Mariotti:2022:WVB**

[MG22] Gianfranco Mariotti and Roberto Giorgi. `WebRISC-V`: a 32/64-bit RISC-V pipeline simulation tool. *SoftwareX*, 18(??):??, June 2022. CODEN ???? ISSN 2352-7110. URL `http://www.sciencedirect.com/science/article/pii/S235271102200070X`.

**Moallemi:2023:SSI**

[MGZ+23] Amirhossein Moallemi, Riccardo Gaspari, Federica Zonzini, Luca De Marchi, Davide Brunelli, and Luca Benini. Speeding up system identification algorithms on a parallel RISC-V MCU for fast near-sensor vibration diagnostic. *IEEE Sensors Letters*, 7(9):1–4, 2023. ISSN 2475-1472.

**Mishra:2022:SVR**

[Mis22] Kishore K. Mishra. *System Verilog with RISC-V Processor Design*. ????, ????, 2022. ???? pp.

**Min:2023:EER**

[MKB+23] Jung Gyu Min, Dongyun Kam, Younghoon Byun, Gunho Park, and Youngjoo Lee. Energy-efficient RISC-V-based vector processor for

cache-aware structurally-pruned transformers. In IEEE, editor, *2023 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Mach:2023:NRV**

[MKČ23] Ján Mach, Lukáš Kohútka, and Pavel Čičák. A new RISC-V CPU for safety-critical systems. In IEEE, editor, *2023 12th Mediterranean Conference on Embedded Computing (MECO)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Madhavan:2020:AVA**

[MKM20] B. Madhavan, A. Kamerish, and R. Manimegalai. ATGP_RISC-V: Automation of test generator using pluggy for RISC-V architecture. In IEEE, editor, *2020 Third International Conference on Smart Systems and Inventive Technology (ICSSIT)*, pages 484–491. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Minev:2023:PCA**

[MKVD23] Petar Minev, Valentina Kukenska, Ilian Varbov, and Matyo Dinev. A practical computer architecture education with RISC-V and TL-Verilog. In IEEE, editor, *2023 XXXII International Scientific Conference Electronics (ET)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Mao:2023:RIR**

[MLD+23] Gaoyu Mao, Yao Liu, Wangchen Dai, Guangyan Li, Zhewen Zhang, Alan H. F. Lam, and Ray C. C. Cheung. REALISE-IoT: RISC-V based efficient and lightweight public-key system for IoT applications. *IEEE Internet of Things Journal*, page 1, 2023. ISSN 2327-4662.

**Ma:2023:DSB**

[MLPH23] Khai-Minh Ma, Duc-Hung Le, Cong-Kha Pham, and Trong-Thuc Hoang. Design of an SoC based on 32-bit RISC-V processor with low-latency lightweight cryptographic cores in FPGA. *Future Internet*, 15(5):186, May 19, 2023. CODEN ???? ISSN 1999-5903. URL `https://www.mdpi.com/1999-5903/15/5/186`.

**Munir:2018:FRV**

[MMA+18] Abdelfattah Munir, Mina Magdy, Samer Ahmed, Sherouk Nasr, Sameh El-Ashry, and Ahmed Shalaby. Fast reliable verification methodology for RISC-V without a reference model. In IEEE, editor, *2018 19th International Workshop on Microprocessor and SOC Test and Verification (MTV)*, pages 12–17. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Mallasen:2022:CCR**

[MMD+22a] David Mallasén, Raul Murillo, Alberto A. Del Barrio, Guillermo Botella, Luis Piñuel, and Manuel Prieto-Matias. Customizing the CVA6 RISC-V core to integrate posit and quire instructions. In IEEE, editor, *2022 37th Conference on Design of Circuits and Integrated Circuits (DCIS)*, pages 01–06. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Mallasen:2022:POSa**

[MMD+22b] David Mallasén, Raul Murillo, Alberto A. Del Barrio, Guillermo Botella, Luis Piñuel, and Manuel Prieto-Matias. PERCIVAL: Open-source posit RISC-V core with quire capability. *IEEE Transactions on Emerging Topics in Computing*, 10(3): 1241–1252, July/September 2022. ISSN 2168-6750 (print), 2376-4562 (electronic).

**Mallasen:2022:POSb**

[MMD+22c] David Mallasén, Raul Murillo, Alberto A. Del Barrio, Guillermo Botella, Luis Piñuel, and Manuel Prieto-Matias. PERCIVAL: Open-source posit RISC-V core with quire capability. In IEEE [IEE22], page 66. ISBN 1-66547-827-6, 1-66547-828-4. LCCN ???? Authors and title only. See [MMD+22b].

**Mantovani:2020:HBR**

[MMGC20] Paolo Mantovani, Robert Margelli, Davide Giri, and Luca P. Carloni. HL5: a 32-bit RISC-V processor designed with high-level synthesis. In IEEE, editor, *2020 IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Menon:2017:SRV**

[MMR+17] A. Menon, S. Murugan, C. Rebeiro, N. Gala, and K. Veezhinathan. Shakti-T: a RISC-V processor with light weight security ex-

tensions. In ACM, editor, *Proceedings of Hardware and Architectural Support for Security and Privacy (HASP), 25 June 2017, Toronto, Canada*, pages 1–8. ACM Press, New York, NY 10036, USA, 2017. ISBN 1-4503-5266-9. URL `https://dl.acm.org/doi/10.1145/3092627.3092629`.

**Martins:2020:BMLa**

[MP20a] J. Martins and S. Pinto. Bao: A modern lightweight embedded hypervisor. In Marko Bertogna and Federico Terraneo, editors, *Workshop on Next Generation Real-Time Embedded Systems (NG-RES 2020)*, pages 3:1–3:14. ????, ????, 2020. URL `https://drops.dagstuhl.de/storage/01oasics/oasics-vol077-ng-res2020/OASIcs.NG-RES.2020.3/OASIcs.NG-RES.2020.3.pdf`.

**Martins:2020:BMLb**

[MP20b] J. Martins and S. Pinto. Bao: A modern lightweight embedded hypervisor. In ????, editor, *Proceedings of the Embedded World Conference, February 2020*, pages 1–5. ????, ????, 2020. URL `https://sandro2pinto.github.io/files/ew2020-bao.pdf`.

**Marshall:2021:LIC**

[MPP21] Ben Marshall, Daniel Page, and Thinh Hung Pham. A lightweight ISE for ChaCha on RISC-V. In IEEE, editor, *2021 IEEE 32nd International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pages 25–32. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Minervini:2023:VAE**

[MPU+23] Francesco Minervini, Oscar Palomar, Osman Unsal, Enrico Reggiani, Josue Quiroga, Joan Marimon, Carlos Rojas, Roger Figueras, Abraham Ruiz, Alberto Gonzalez, Jonnatan Mendoza, Ivan Vargas, César Hernandez, Joan Cabre, Lina Khoirunisya, Mustapha Bouhali, Julian Pavon, Francesc Moll, Mauro Olivieri, Mario Kovac, Mate Kovac, Leon Dragic, Mateo Valero, and Adrian Cristal. Vitruvius+: an area-efficient RISC-V decoupled vector coprocessor for high performance computing applications. *ACM Transactions on Architecture and Code Optimization*, 20(2):28:1–28:??, June 2023. CODEN ???? ISSN 1544-3566 (print), 1544-3973 (electronic). URL `https://dl.acm.org/doi/10.1145/3575861`.

**Markov:2022:IRV**

[MR22] D. Markov and A. Romanov. Implementation of the RISC-V architecture with the extended Zbb instruction set. In IEEE, editor, *2022 International Ural Conference on Electrical Power Engineering (UralCon)*, pages 180–184. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Molina-Robles:2023:ECB**

[MRAM+23] Roberto Molina-Robles, Alfredo Arnaud, Matías Miguez, Joel Gak, Alfonso Chacón-Rodríguez, and Ronny García-Ramírez. An energy consumption benchmark for a low-power RISC-V core aimed at implantable medical devices. *IEEE Embedded Systems Letters*, 15(2):57–60, 2023. ISSN 1943-0663 (print), 1943-0671 (electronic).

**Morris:2023:EDA**

[MRB+23] Jordan Morris, Ashur Rafiev, Graeme M. Bragg, Mark L. Vousden, David B. Thomas, Alex Yakovlev, and Andrew D. Brown. An event-driven approach to genotype imputation on a custom RISC-V cluster. *IEEE/ACM Transactions on Computational Biology and Bioinformatics*, pages 1–10, 2023. CODEN ITCBCY. ISSN 1545-5963 (print), 1557-9964 (electronic).

**Morris:2024:EDA**

[MRB+24] Jordan Morris, Ashur Rafiev, Graeme M. Bragg, Mark L. Vousden, David B. Thomas, Alex Yakovlev, and Andrew D. Brown. An event-driven approach to genotype imputation on a custom RISC-V cluster. *IEEE/ACM Transactions on Computational Biology and Bioinformatics*, 21(1):26–35, 2024. CODEN ITCBCY. ISSN 1545-5963 (print), 1557-9964 (electronic). URL `https://dl.acm.org/doi/10.1109/TCBB.2023.3328714`.

**Molina-Robles:2021:APS**

[MRGRCR+21a] Roberto Molina-Robles, Ronny García-Ramírez, Alfonso Chacón-Rodríguez, Renato Rimolo-Donadio, and Alfredo Arnaud. An affordable post-silicon testing framework applied to a RISC-V based microcontroller. In IEEE, editor, *2021 IEEE Latin America Electron Devices Conference (LAEDC)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Molina-Robles:2021:LLA**

[MRGRCR+21b] Roberto Molina-Robles, Ronny García-Ramírez, Al-

fonso Chacón-Rodríguez, Renato Rimolo-Donadio, and Alfredo Arnaud. Low-level algorithm for a software-emulated $I^2C$ I/O module in general purpose RISC-V based microcontrollers. In IEEE, editor, *2021 IEEE URUCON*, pages 90–94. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Molina-Robles:2020:CFV**

[MRSBGR+20] Roberto Molina-Robles, Edgar Solera-Bolanos, Ronny García-Ramírez, Alfonso Chacón-Rodríguez, Alfredo Arnaud, and Renato Rimolo-Donadio. A compact functional verification flow for a RISC-V 32I based core. In IEEE, editor, *2020 IEEE 3rd Conference on PhD Research in Microelectronics and Electronics in Latin America (PRIME-LA)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Matthews:2017:TNR**

[MS17] Eric Matthews and Lesley Shannon. TAIGA: a new RISC-V soft-processor framework enabling high performance CPU architectural features. In IEEE, editor, *2017 27th International Conference on Field Programmable Logic and Applications (FPL)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017.

**Mezger:2022:SRV**

[MSD+22] Benjamin W. Mezger, Douglas A. Santos, Luigi Dilillo, Cesar A. Zeferino, and Douglas R. Melo. A survey of the RISC-V architecture software support. *IEEE Access*, 10:51394–51411, 2022. ISSN 2169-3536.

**Mezger:2023:HRT**

[MSDM23] Benjamin W. Mezger, Douglas A. Santos, Luigi Dilillo, and Douglas R. Melo. Hardening a real-time operating system for a dependable RISC-V System-on-Chip. In IEEE, editor, *2023 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Mueller:2021:RVB**

[MSFK21] Kai-Uwe Mueller, Alexander Stanitzki, Tatjana Fedtschenko, and Rainer Kokozinski. RISC-V based SoC with integrated switched-capacitor PUF in 180 nm. In IEEE, editor, *MikroSystemTechnik Congress 2021;*

*Congress*, pages 1–3. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**McGrew:2019:FTU**

[MSJ19] Tyler McGrew, Eric Schonauer, and Peter Jamieson. Framework and tools for undergraduates designing RISC-V processors on an FPGA in computer architecture education. In IEEE, editor, *2019 International Conference on Computational Science and Computational Intelligence (CSCI)*, pages 778–781. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Malone:2023:RVP**

[MSP23] Steven Malone, Patrick Saenz, and Patrick Phelan. RISC-V processors for spaceflight embedded platforms. In IEEE, editor, *2023 IEEE Aerospace Conference*, pages 1–11. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Merchant:2021:AFB**

[MSR+21] Farhad Merchant, Dominik Sisejkovic, Lennart M. Reimann, Kirthihan Yasotharan, Thomas Grass, and Rainer Leupers. ANDROMEDA: an FPGA based RISC-V MPSoC exploration framework. In IEEE, editor, *2021 34th International Conference on VLSI Design and 2021 20th International Conference on Embedded Systems (VLSID)*, pages 270–275. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Malathi:2023:DRV**

[MSSS23] D. Malathi, R. Sneha, M. Shanmugapriya, and S. Sethurajan. Design of RISC-V processing unit using posit number system. In IEEE, editor, *2023 4th International Conference on Signal Processing and Communication (ICSPC)*, pages 427–431. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Mendat:2023:RVN**

[MST+23] Daniel R. Mendat, Jonah P. Sengupta, Gaspar Tognetti, Martin Villemur, Philippe O. Pouliquen, Sergio Montano, Kayode Sanni, Jamal L. Molin, Nishant Zachariah, Isidoros Doxas, and Andreas G. Andreou. A RISC-V neuromorphic microcontroller unit (vMCU) with event-based physical interface and computational memory for low-latency machine perception and intelli-

gence at the edge. In IEEE, editor, *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Mach:2019:FSB**

[MSZB19] Stefan Mach, Fabian Schuiki, Florian Zaruba, and Luca Benini. A 0.80pJ/flop, 1.24Tflop/sW 8-to-64 bit transprecision floating-point unit for a 64 bit RISC-V processor in 22nm FD-SOI. In IEEE, editor, *2019 IFIP/IEEE 27th International Conference on Very Large Scale Integration (VLSI-SoC)*, pages 95–98. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Martinoli:2022:RIC**

[MTAL22] Valentin Martinoli, Yannick Teglia, Bouagoun Abdellah, and Régis Leveugle. Recovering information on the CVA6 RISC-V CPU with a baremetal micro-architectural covert channel. In IEEE, editor, *2022 IEEE 28th International Symposium on On-Line Testing and Robust System Design (IOLTS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Mao:2021:CEB**

[MTCL21] Binjie Mao, Nianxiong Tan, Ting Chong, and Lei Li. A CLIC extension based fast interrupt system for embedded RISC-V processors. In IEEE, editor, *2021 6th International Conference on Integrated Circuits and Microsystems (ICICM)*, pages 109–113. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Moratelli:2022:MRV**

[MTJ+22] Carlos Moratelli, Ramão Tiburski, Sérgio F. Johann, Emanuel Moura, Everton De Matos, and Fabiano Hessel. MIPS and RISC-V: Evaluating virtualization trade-off for edge devices. In IEEE, editor, *2022 IEEE 8th World Forum on Internet of Things (WF-IoT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Matsuno:2021:RWE**

[MTT21] Shota Matsuno, Masashi Tawada, and Nozomu Togawa. Reducing writing energy consumption for non-volatile registers utilizing frequent patterns of sequential bits on RISC-V ar-

chitecture. In IEEE, editor, *2021 IEEE International Conference on Consumer Electronics (ICCE)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Meng:2022:DBH**

[MZZG22] Ziqin Meng, Yunrui Zhang, Jianyang Zhou, and Zichao Guo. Design of 64-bit high-performance embedded processor supporting RISC-V B-extension. In IEEE, editor, *2022 IEEE 16th International Conference on Anti-counterfeiting, Security, and Identification (ASID)*, pages 28–32. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Ng:2022:RIP**

[NAL22] Jien Hau Ng, Chee Hong Ang, and Hwa Chaw Law. A realization of IO physical memory protection for RISC-V systems. In IEEE, editor, *2022 IEEE 15th International Symposium on Embedded Multicore/Manycore Systems-on-Chip (MCSoC)*, pages 375–380. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Nguyen:2022:TNN**

[NBT22] Ngo-Doanh Nguyen, Duy-Hieu Bui, and Xuan-Tu Tran. Tiny neuron network system based on RISC-V processor: a decentralized approach for IoT applications. In IEEE, editor, *2022 International Conference on Advanced Technologies for Communications (ATC)*, pages 98–103. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Nannipieri:2021:RVP**

[NDZ+21] Pietro Nannipieri, Stefano Di Matteo, Luca Zulberti, Francesco Albicocchi, Sergio Saponara, and Luca Fanucci. A RISC-V post quantum cryptography instruction set extension for number theoretic transform to speed-up CRYSTALS algorithms. *IEEE Access*, 9: 150798–150808, 2021. ISSN 2169-3536.

**Nicholas:2020:SAS**

[NGS20] Geraldine Shirley Nicholas, Yutian Gui, and Fareena Saqib. A survey and analysis on SoC platform security in ARM, Intel and RISC-V architecture. In IEEE, editor, *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 718–721. IEEE Computer

Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Nguyen-Hoang:2022:IBR**

[NHML+22] Duc-Thinh Nguyen-Hoang, Khai-Minh Ma, Duy-Linh Le, Hong-Hai Thai, Tran-Bao-Thuong Cao, and Duc-Hung Le. Implementation of a 32-bit RISC-V processor with cryptography accelerators on FPGA and ASIC. In IEEE, editor, *2022 IEEE Ninth International Conference on Communications and Electronics (ICCE)*, pages 219–224. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Nguyen:2021:CBT**

[NKH+21] Khai-Duy Nguyen, Dang Tuan Kiet, Trong-Thuc Hoang, Nguyen Quang Nhu Quynh, and Cong-Kha Pham. A CORDIC-based trigonometric hardware accelerator with custom instruction in 32-bit RISC-V System-on-Chip. In IEEE, editor, *2021 IEEE Hot Chips 33 Symposium (HCS)*, pages 1–13. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Nikiema:2023:DLC**

[NKTS23] Pegdwende Romaric Nikiema, Angeliki Kritikakou, Marcello Traiola, and Olivier Sentieys. Design with low complexity fine-grained Dual Core Lock-Step (DCLS) RISC-V processors. In IEEE, editor, *2023 53rd Annual IEEE/IFIP International Conference on Dependable Systems and Networks — Supplemental Volume (DSN-S)*, pages 224–229. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Nanjundaswamy:2023:RVT**

[NNPG23] Nithin Ravani Nanjundaswamy, Gregor Nitsche, Frank Poppen, and Kim Grüttner. RISC-V timing-instructions for open time-triggered architectures. In IEEE, editor, *2023 53rd Annual IEEE/IFIP International Conference on Dependable Systems and Networks Workshops (DSN-W)*, pages 211–214. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Nikiema:2023:TDR**

[NPA+23] Pegdwende Romaric Nikiema, Alessandro Palumbo, Allan Aasma, Luca Cassano, Angeliki Kritikakou, Ari Kulmala, Jari Lukkarila, Marco Ottavi, Rafail Psiakis, and Marcello Traiola. Towards

dependable RISC-V cores for edge computing devices. In IEEE, editor, *2023 IEEE 29th International Symposium on On-Line Testing and Robust System Design (IOLTS)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Nair:2022:HIN**

[NRA+22] M. K. Aparna Nair, Police Manoj Kumar Reddy, Y. L. Abijith, Venkatesh Rajagopalan, and J. Soumya. Hardware implementation of network interface architecture for RISC-V based NoC-MPSoC framework. In IEEE, editor, *2022 35th International Conference on VLSI Design and 2022 21st International Conference on Embedded Systems (VLSID)*, pages 86–91. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Nadalini:2023:TWR**

[NRB+23] Alessandro Nadalini, Georg Rutishauser, Alessio Burrello, Nazareno Bruschi, Angelo Garofalo, Luca Benini, Francesco Conti, and Davide Rossi. A 3 TOPS/W RISC-V parallel cluster for inference of fine-grain mixed-precision quantized neural networks. In IEEE, editor, *2023 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Nurmi:2022:RSD**

[NRLH22] Antti Nurmi, Antti Rautakoura, Henri Lunnikivi, and Timo D. Hämäläinen. A resilient system design to boot a RISC-V MPSoC. In IEEE, editor, *2022 25th Euromicro Conference on Digital System Design (DSD)*, pages 232–238. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Nunes:2023:VAA**

[NSM+23] Willian Analdo Nunes, Marcos Luiggi Lemos Sartori, Matheus Trevisan Moreira, Fernando Gehm Moraes, and Ney Laert Vilar Calazans. Validating an automated asynchronous synthesis environment with a challenging design: RISC-V. In IEEE, editor, *2023 36th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Nascimento:2023:RVS**

[NWP+23] Felipe F. Nascimento, Rodrigo N. Wuerdig, André F. Ponchet, Bruno Sanches, Denis S. Loubach, Roberto D'Amore, Marcus H. Victor Junior, Walter S. Oliveira, Vitor O. Kuribara, and Luiz C. Moreira. RISC-V SoC physical implementation in 180 nm CMOS with a Quark core based on FemtoRV32. In IEEE, editor, *2023 IEEE Seventh Ecuador Technical Chapters Meeting (ECTM)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Ottaviano:2024:CRV**

[OBB+24] Alessandro Ottaviano, Robert Balas, Giovanni Bambini, Antonio Del Vecchio, Maicol Ciani, Davide Rossi, Luca Benini, and Andrea Bartolini. ControlPULP: a RISC-V on-chip parallel power controller for many-core HPC processors with FPGA-based hardware-in-the-loop power and thermal emulation. *International Journal of Parallel Programming*, 52 (1–2):93–123, April 2024. CODEN IJPPE5. ISSN 0885-7458 (print), 1573-7640 (electronic). URL `https://link.springer.com/article/10.1007/s10766-024-00761-4`.

**Ottaviano:2023:CLL**

[OBSB23] Alessandro Ottaviano, Thomas Benz, Paul Scheffler, and Luca Benini. Cheshire: a lightweight, Linux-capable RISC-V host platform for domain-specific accelerator plug-in. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 70 (10):3777–3781, 2023. ISSN 1549-7747 (print), 1558-3791 (electronic).

**Olivieri:2017:IOP**

[OCC+17] Mauro Olivieri, Abdallah Cheikh, Gianmarco Cerutti, Antonio Mastrandrea, and Francesco Menichelli. Investigation on the optimal pipeline organization in RISC-V multi-threaded soft processor cores. In IEEE, editor, *2017 New Generation of CAS (NGCAS)*, pages 45–48. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017.

**Oleksiak:2019:DVE**

[OCMP19] Adrian Oleksiak, Sebastian Cieślak, Krzysztof Marcinek, and Witold A. Pleskacz. Design and verification environment for RISC-V processor cores. In IEEE, editor, *2019 MIXDES — 26th International Conference "Mixed Design of Integrated Circuits and Systems"*, pages

206–209. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Ottavi:2020:MPR**

[OGT+20] Gianmarco Ottavi, Angelo Garofalo, Giuseppe Tagliavini, Francesco Conti, Luca Benini, and Davide Rossi. A mixed-precision RISC-V processor for extreme-edge DNN inference. In IEEE, editor, *2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pages 512–517. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Oh:2018:DGS**

[OPY+18] Hyunyoung Oh, Junmo Park, Myonghoon Yang, Dongil Hwang, and Yunheung Paek. Design of a generic security interface for RISC-V processors and its applications. In IEEE, editor, *2018 International SoC Design Conference (ISOCC)*, pages 40–41. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Paulin:2021:RBR**

[PACB21] Gianna Paulin, Renzo Andri, Francesco Conti, and Luca Benini. RNN-based radio resource management on multicore RISC-V accelerator architectures. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 29(9):1624–1637, 2021. CODEN IEVSE9. ISSN 1063-8210 (print), 1557-9999 (electronic).

**Parvin:2023:RDL**

[PAPJ+23] Sajjad Parvin, Sallar Ahmadi-Pour, Chandan Kumar Jha, Frank Sill Torres, and Rolf Drechsler. Lo-RISK: Design of a low optical leakage and high performance RISC-V core. In IEEE, editor, *2023 IEEE International Conference on Omni-layer Intelligent Systems (COINS)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Patterson:2017:RIS**

[Pat17] David Patterson. Reduced instruction set computers then and now. *Computer*, 50 (12):10–12, December 2017. CODEN CPTRB4. ISSN 0018-9162 (print), 1558-0814 (electronic). URL `https://www.computer.org/csdl/mags/co/2017/12/mco2017120010.html`.

**Patterson:2018:YCA**

[Pat18] David Patterson. 50 years of computer architecture: From the mainframe CPU to the domain-specific TPU

and the open RISC-V instruction set. In IEEE, editor, *2018 IEEE International Solid-State Circuits Conference — (ISSCC)*, pages 27–31. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Perotti:2024:AES**

[PCA+24] Matteo Perotti, Matheus Cavalcante, Renzo Andri, Lukas Cavigelli, and Luca Benini. Ara2: Exploring single- and multi-core vector processing with an efficient RVV 1.0 compliant open-source processor. *IEEE Transactions on Computers*, 73(7):1822–1836, July 2024. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Park:2023:DUL**

[PCL+23] Jina Park, Eunjin Choi, Kyungwon Lee, Jae-Jin Lee, Kyuseung Han, and Woojoo Lee. Developing an ultra-low power RISC-V processor for anomaly detection. In IEEE, editor, *2023 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1–2. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Perotti:2023:YOS**

[PCO+23] Matteo Perotti, Matheus Cavalcante, Alessandro Ottaviano, Jiantao Liu, and Luca Benini. Yun: an open-source, 64-bit RISC-V-based vector processor with multi-precision integer and floating-point support in 65-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 70(10):3732–3736, 2023. ISSN 1549-7747 (print), 1558-3791 (electronic).

**Perotti:2022:NAV**

[PCW+22] Matteo Perotti, Matheus Cavalcante, Nils Wistoff, Renzo Andri, Lukas Cavigelli, and Luca Benini. A "New Ara" for vector computing: an open source highly efficient RISC-V V 1.0 vector processor design. In IEEE, editor, *2022 IEEE 33rd International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pages 43–51. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Palmiero:2018:DID**

[PDLC18] Christian Palmiero, Giuseppe Di Guglielmo, Luciano Lavagno, and Luca P. Carloni. Design and implementation of a dynamic infor-

mation flow tracking architecture to secure a RISC-V core for IoT applications. In IEEE, editor, *2018 IEEE High Performance extreme Computing Conference (HPEC)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Perez:2021:COS**

[PFD21] Boria Perez, Alexander Fell, and John D. Davis. Coyote: an open source simulation tool to enable RISC-V in HPC. In IEEE, editor, *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 130–135. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Parvin:2023:TDP**

[PGTD23] Sajjad Parvin, Mehran Goli, Frank Sill Torres, and Rolf Drechsler. Trojan-D2: Post-layout design and detection of stealthy hardware trojans — a RISC-V case study. In IEEE, editor, *2023 28th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages 683–689. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Petrisko:2020:BAO**

[PGW+20] Daniel Petrisko, Farzam Gilani, Mark Wyse, Dai Cheol Jung, Scott Davidson, Paul Gao, Chun Zhao, Zahra Azad, Sadullah Canakci, Bandhav Veluri, Tavio Guarino, Ajay Joshi, Mark Oskin, and Michael Bedford Taylor. BlackParrot: an agile open-source RISC-V multicore for accelerator SoCs. *IEEE Micro*, 40(4): 93–102, July/August 2020. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

**Pircher:2021:ERV**

[PGZMG21] S. Pircher, J. Geier, A. Zeh, and D. Mueller-Gritschneder. Exploring the RISC-V vector extension for the classic McEliece post-quantum cryptosystem. In IEEE, editor, *2021 22nd International Symposium on Quality Electronic Design (ISQED)*, pages 401–407. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Patterson:2017:COD**

[PH17] David A. Patterson and John L. Hennessy. *Computer Organization and Design: the Hardware/Software Interface*. Morgan Kaufmann series in computer architecture and design. Morgan Kaufmann

Publishers, Cambridge, MA, USA / Amsterdam, The Netherlands /, RISC-V edition, 2017. ISBN 0-12-812275-7 (paperback), 0-12-812276-5 (e-book). xxiv + 565 + a-86 + i + 22 pp. LCCN QA76.9.C643.

**Pekkarinen:2018:MRV**

[PH18] Esko Pekkarinen and Timo D. Hämäläinen. Modeling RISC-V processor in IP-XACT. In IEEE, editor, *2018 21st Euromicro Conference on Digital System Design (DSD)*, pages 140–147. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Patterson:2021:COD**

[PH21] David A. Patterson and John L. Hennessy. *Computer Organization and Design: the Hardware Software Interface*. Morgan Kaufmann Publishers, Cambridge, MA, USA / Amsterdam, The Netherlands /, second RISC-V edition, 2021. ISBN 0-12-820331-5. xx + 712 pp. LCCN QA76.9.C643 P373 2021.

**Park:2023:FDL**

[PHC+23] Jina Park, Kyuseung Han, Eunjin Choi, Sukho Lee, Jae-Jin Lee, Woojoo Lee, and Massoud Pedram. Florian: Developing a low-power RISC-V multicore processor with a shared lightweight FPU. In IEEE, editor, *2023 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Papaphilippou:2021:SRV**

[PJL21] Philippos Papaphilippou, Kelly Paul H. J., and Wayne Luk. Simodense: a RISC-V softcore optimised for exploring custom SIMD instructions. In IEEE, editor, *2021 31st International Conference on Field-Programmable Logic and Applications (FPL)*, pages 391–397. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Park:2020:DFA**

[PKC+20] Heechun Park, Jinwoo Kim, Venkata Chaitanya Krishna Chekuri, Majid Ahadi Dolatsara, Mohammed Nabeel, Alabi Bojesomo, Satwik Patnaik, Ozgur Sinanoglu, Madhavan Swaminathan, Saibal Mukhopadhyay, Johann Knechtel, and Sung Kyu Lim. Design flow for active interposer-based 2.5-d ICs and study of RISC-V architecture with secure NoC. *IEEE Transactions*

*on Components, Packaging and Manufacturing Technology*, 10(12):2047–2060, 2020. CODEN ITCPC8. ISSN 2156-3950 (print), 2156-3985 (electronic).

**Park:2022:BIS**

[PKKK22] Seonghwan Park, Dongwook Kang, Jeonghwan Kang, and Donghyun Kwon. Bratter: An instruction set extension for forward control-flow integrity in RISC-V. *Sensors (Basel)*, 27(4):1392–1405, February 2022. CODEN SENSC9. ISSN 1424-8220.

**Papaphilippou:2021:DCS**

[PKL21] Philippos Papaphilippou, Paul H. J. Kelly, and Wayne Luk. Demonstrating custom SIMD instruction development for a RISC-V softcore. In IEEE, editor, *2021 31st International Conference on Field-Programmable Logic and Applications (FPL)*, page 139. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Papadopoulos:2020:CTH**

[PKN+20] Nikolaos Charalampos Papadopoulos, Vasileios Karakostas, Konstantinos Nikas, Nectarios Koziris, and Dionisios N. Pnevmatikatos. A configurable TLB hierarchy for the RISC-V architecture. In IEEE, editor, *2020 30th International Conference on Field-Programmable Logic and Applications (FPL)*, pages 85–90. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Pan:2022:PCA**

[PLH+22] Sing-Yu Pan, Shuenn-Yuh Lee, Yi-Wen Hung, Chou-Ching Lin, and Gia-Shing Shieh. A programmable CNN accelerator with RISC-V core in real-time wearable application. In IEEE, editor, *2022 IEEE International Conference on Recent Advances in Systems Science and Engineering (RASSE)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Pnevmatikou:2020:FPC**

[PLSK20] Arsinoe Pnevmatikou, George Lentaris, Dimitrios Soudris, and Nikos Kokkalis. Fast packet classification using RISC-V and HyperSplit acceleration on FPGA. In IEEE, editor, *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Porter:2019:ESC**

[PMBA19] Ross Porter, Sam Morgan, and Morteza Biglari-Abhari. Extending a soft-core RISC-V processor to accelerate CNN inference. In IEEE, editor, *2019 International Conference on Computational Science and Computational Intelligence (CSCI)*, pages 694–697. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Phangestu:2022:FSP**

[PMKZ22] Aaron Elson Phangestu, Ir. Totok Mujiono, M. I. Kom, and St Ahmad Zaini. Five-stage pipelined 32-bit RISC-V base integer instruction set architecture soft microprocessor core in VHDL. In IEEE, editor, *2022 International Seminar on Intelligent Technology and Its Applications (ISITIA)*, pages 304–309. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Poorhosseini:2020:CCR**

[PNG20] Mehrdad Poorhosseini, Wolfgang Nebel, and Kim Grüttner. A compiler comparison in the RISC-V ecosystem. In IEEE, editor, *2020 International Conference on Omni-layer Intelligent Systems (COINS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Patsidis:2020:RVS**

[PNSD20] Kariofyllis Patsidis, Chrysostomos Nicopoulos, Georgios Ch. Sirakoulis, and Giorgos Dimitrakopoulos. RISC-V$^2$: a scalable RISC-V vector processor. In IEEE, editor, *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Prabhakaran:2022:DAM**

[PNV22] Sandeep Prabhakaran, Mathan N, and V. Vedanarayanan. Design and analysis of a multi clocked pipelined processor based on RISC-V. In IEEE, editor, *2022 International Conference on Communication, Computing and Internet of Things (IC3IoT)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Plusquellic:2022:ILA**

[POMD22] Jim Plusquellic, Donald E. Owen, Tom J. Mannos, and Brian Dziki. Information leakage analysis using a co-design-based fault injection

technique on a RISC-V microprocessor. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 41(3): 438–451, 2022. CODEN ITCSDI. ISSN 0278-0070 (print), 1937-4151 (electronic).

**Payvar:2019:IER**

[PPS+19] Saman Payvar, Esko Pekkarinen, Rafael Stahl, Daniel Mueller-Gritschneder, and Timo D. Hämäläinen. Instruction extension of a RISC-V processor modeled with IP-XACT. In IEEE, editor, *2019 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Philip:2023:ICE**

[PPYB23] Sebin Shaji Philip, Roberto Passerone, Kasim Sinan Yildirim, and Davide Brunelli. Intermittent computing emulation of ultralow-power processors: Evaluation of backup strategies for RISC-V. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 42(1):82–94, 2023. CODEN ITCSDI. ISSN 0278-0070 (print), 1937-4151 (electronic).

**Pillement:2023:SRV**

[PRP+23] S. Pillement, M. Méndez Real, J. Pottier, T. Nieddu, B. Le Gal, S. Faucou, J. L. Béchennec, M. Briday, S. Girbal, J. Le Rhun, O. Gilles, D. Gracia Pérez, A. Sintzoff, and J. R. Coulon. Securing a RISC-V architecture: a dynamic approach. In IEEE, editor, *2023 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Patil:2015:OFP**

[PRS+15] Vinayak Patil, Aneesh Raveendran, P. M. Sobha, A. David Selvakumar, and D. Vivian. Out of order floating point coprocessor for RISC V ISA. In IEEE, editor, *2015 19th International Symposium on VLSI Design and Test*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2015.

**Paludo:2022:NAL**

[PS22a] Rogério Paludo and Leonel Sousa. NTT architecture for a Linux-ready RISC-V fully-homomorphic encryption accelerator. *IEEE*

*Transactions on Circuits and Systems I: Regular Papers*, 69(7):2669–2682, 2022. ISSN 1549-8328 (print), 1558-0806 (electronic).

**Popovici:2022:ERV**

[PS22b] Cosmin-Andrei Popovici and Andrei Stan. Extending a RISC-V core with a CAN-FD communication unit. In IEEE, editor, *2022 26th International Conference on System Theory, Control and Computing (ICSTCC)*, pages 31–36. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Popovici:2023:RVE**

[PSM23] Cosmin-Andrei Popovici, Andrei Stan, and Vasile-Ion Manta. RISC-V extension for optimized PWM control. In IEEE, editor, *2023 27th International Conference on System Theory, Control and Computing (ICSTCC)*, pages 404–409. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**P:2023:AOF**

[PSS23] Gayathri G P, Jaya S, and Krishnakumar Rao S. An area optimized floating-point coprocessor for RISC-V processor. In IEEE, editor, *2023 International Conference on Control, Communication and Computing (ICCC)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Poli:2021:DIR**

[PSZMM21] Ludovico Poli, Sangeet Saha, Xiaojun Zhai, and Klaus D. Mcdonald-Maier. Design and implementation of a RISC V processor on FPGA. In IEEE, editor, *2021 17th International Conference on Mobility, Sensing and Networking (MSN)*, pages 161–166. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Patterson:2017:RVR**

[PW17a] David Patterson and Andrew Waterman. *The RISC-V Reader: an Open Architecture Atlas*. Strawberry Canyon, San Francisco, CA, USA, 2017. ISBN 0-9992491-1-8. xiv + 180 pp. LCCN QA76.9.A73 P388 2017.

**Patterson:2017:SIC**

[PW17b] David Patterson and Andrew Waterman. SIMD instructions considered harmful. ACM Web site, September 18, 2017. URL `https://www.sigarch.org/simd-`

`instructions-considered-harmful/`.

**Qi:2023:DPF**

[QCL+23] Yu Qi, Mengxue Chen, Guilan Li, Gaosheng Li, Meisheng He, and Bangjian Xu. A deeply pipelined FMA unit for high performance RISC-V processor. In IEEE, editor, *2023 2nd International Conference on Computing, Communication, Perception and Quantum Technology (CCPQT)*, pages 53–59. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Qui:2020:DIB**

[QLC20] Nguyen My Qui, Chang Hong Lin, and Poki Chen. Design and implementation of a 256-bit RISC-V-based dynamically scheduled very long instruction word on FPGA. *IEEE Access*, 8: 172996–173007, 2020. ISSN 2169-3536.

**Qin:2021:CHA**

[QLH21] Xinyu Qin, Xudong Liu, and Jun Han. A CNN hardware accelerator designed for YOLO algorithm based on RISC-V SoC. In IEEE, editor, *2021 IEEE 14th International Conference on ASIC (ASICON)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Qiu:2021:AVP**

[QYZ21] Jing Qiu, Fei Ye, and Hua Zhou. Automatic verification platform based on RISC-V architecture microprocessor. In IEEE, editor, *2021 International Conference on Networking Systems of AI (INSAI)*, pages 157–160. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Rajagopal:2021:EQE**

[Raj21] S. Rajagopal. EDGE Q 5G with an EDGE. In IEEE, editor, *Proceedings of the IEEE Hot Chips 33 Symposium (HCS), August 2021*, pages 1–13. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Rao:2023:IRE**

[RAPK23] Ambika S. Rao, Rahul Anilkumar, K. Padmapriya, and K. Sudeendra Kumar. Improving reliability of embedded RISC-V SoC for low-cost space applications. In IEEE, editor, *2023 International Conference on Networking and Communications (ICNWC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street,

Suite 300, Silver Spring, MD 20910, USA, 2023.

**Richmond:2018:ECT**

[RBK18] Dustin Richmond, Michael Barrow, and Ryan Kastner. Everyone's a critic: a tool for exploring RISC-V projects. In IEEE, editor, *2018 28th International Conference on Field Programmable Logic and Applications (FPL)*, pages 260–2604. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Rostami:2024:FEH**

[RCK+24] Mohamadreza Rostami, Chen Chen, Rahul Kande, Huimin Li, Jeyavijayan Rajendran, and Ahmad-Reza Sadeghi. Fuzzerfly effect: Hardware fuzzing for memory safety. *IEEE Security & Privacy*, 22(4):76–86, July/August 2024. ISSN 1540-7993 (print), 1558-4046 (electronic).

**Ramirez:2024:PGB**

[RCMQO24] Cristian Ramírez, Adrián Castelló, Héctor Martínez, and Enrique S. Quintana-Ortí. Parallel GEMM-based convolution for deep learning on multicore RISC-V processors. *The Journal of Supercomputing*, 80(9): 12623–12643, June 2024. CODEN JOSUED. ISSN 0920-8542 (print), 1573-0484 (electronic). URL `https://link.springer.com/article/10.1007/s11227-024-05927-y`.

**Ruospo:2019:LTA**

[RCS+19] Annachiara Ruospo, Riccardo Cantoro, Ernesto Sanchez, Pasquale Davide Schiavone, Angelo Garofalo, and Luca Benini. Online testing for autonomous systems driven by RISC-V processor design verification. In IEEE, editor, *2019 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Roy:2020:EHS**

[RFS20] Debapriya Basu Roy, Tim Fritzmann, and Georg Sigl. Efficient hardware/software co-design for post-quantum crypto algorithm SIKE on ARM and RISC-V based microcontrollers. In IEEE, editor, *2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, pages 1–9. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Rutishauser:2023:CMR**

[RHD+23] Georg Rutishauser, Robin Hunziker, Alfio Di Mauro, Sizhen Bian, Luca Benini, and Michele Magno. ColibriES: a milliwatts RISC-V based embedded system leveraging neuromorphic and neural networks hardware accelerators for low-latency closed-loop control applications. In IEEE, editor, *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Riese:2021:MTP**

[RHGD21] Frank Riese, Vladimir Herdt, Daniel Große, and Rolf Drechsler. Metamorphic testing for processor verification: a RISC-V case study at the instruction level. In IEEE, editor, *2021 IFIP/IEEE 29th International Conference on Very Large Scale Integration (VLSI-SoC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Ramsauer:2022:SHP**

[RHS+22] Ralf Ramsauer, Stefan Huber, Konrad Schwarz, Jan Kiszka, and Wolfgang Mauerer. Static hardware partitioning on RISC-V: Shortcomings, limitations, and prospects. In IEEE, editor, *2022 IEEE 8th World Forum on Internet of Things (WF-IoT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Rogan:2023:RVI**

[RK23] Sam Rogan and Yoshihito Kondo. RISC-V is inevitable. In IEEE, editor, *2023 International Conference on IC Design and Technology (ICICDT)*, page xxxvi. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Rao:2023:GBC**

[RKH+23] Ambika S. Rao, Arjun Kudtarkar, Lakshmi Harakuni, G. Nagendra Rao, and Kumar K. Sudeendra. A generic on-board computer based on RISC-V architecture processor for low cost nanosatellite applications. In IEEE, editor, *2023 2nd International Conference on Vision Towards Emerging Trends in Communication and Networking Technologies (ViTECoN)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Reichenbach:2021:RVR**

[RKRF21] Marc Reichenbach, Johannes Knödtel, Sebastian Rachuj, and Dietmar Fey. RISC-V3: a RISC-V compatible CPU with a data path based on redundant number systems. *IEEE Access*, 9:43684–43700, 2021. ISSN 2169-3536.

**Richter:2021:RVB**

[RLL+21] Mike Richter, Andre Luedecke, Yoon-Cue Lee, Alexander Stanitzki, Alexander Utz, Guenter Grau, Holger Kappert, and Rainer Kokozinski. A RISC-V-based system on chip for high-speed control in safety-critical 650 V GaN-Applications. In IEEE, editor, *SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Razilov:2022:CSP**

[RMF22] Viktor Razilov, Emil Matúš, and Gerhard Fettweis. Communications signal processing using RISC-V vector extension. In IEEE, editor, *2022 International Wireless Communications and Mobile Computing (IWCMC)*, pages 690–695. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Rodrigues:2019:THF**

[RMP+19] Cristiano Rodrigues, Ivo Marques, Sandro Pinto, Tiago Gomes, and Adriano Tavares. Towards a heterogeneous fault-tolerance architecture based on Arm and RISC-V processors. In IEEE, editor, *IECON 2019 — 45th Annual Conference of the IEEE Industrial Electronics Society*, volume 1, pages 3112–3117. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Rojas:2021:LCB**

[RMR21] Camilo Rojas, Hanssel Morales, and Elkim Roa. A low-cost bug hunting verification methodology for RISC-V-based processors. In IEEE, editor, *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Rotar:2022:RVB**

[RPA22] Danut Rotar, Teodor Petriţa, and Florin Alexa. RISC-V based HW accelerator. In IEEE, editor, *2022 International Symposium on Electronics and Telecommuni-*

*cations (ISETC)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Raveendran:2015:RVO**

[RPD+15] Aneesh Raveendran, Vinayak Patil, Vivian Desalphine, P. M. Sobha, and A. David Selvakumar. RISC-V out-of-order data conversion co-processor. In IEEE, editor, *2015 19th International Symposium on VLSI Design and Test*, pages 1–2. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2015.

**Raveendran:2016:RVI**

[RPSD16] Aneesh Raveendran, Vinayak Baramu Patil, David Selvakumar, and Vivian Desalphine. A RISC-V instruction set processor-micro-architecture design and analysis. In IEEE, editor, *2016 International Conference on VLSI Systems, Architectures, Technology and Applications (VLSI-SATA)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2016.

**Ravaglia:2020:MLA**

[RRC+20] Leonardo Ravaglia, Manuele Rusci, Alessandro Capotondi, Francesco Conti, Lorenzo Pellegrini, Vincenzo Lomonaco, Davide Maltoni, and Luca Benini. Memory-latency-accuracy trade-offs for continual learning on a RISC-V extreme-edge node. In IEEE, editor, *2020 IEEE Workshop on Signal Processing Systems (SiPS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Rajabalipanah:2021:ARV**

[RRJ+21] Maryam Rajabalipanah, Mahboobe Sadeghipour Roodsari, Zahra Jahanpeima, Gianluca Roascio, Paolo Prinetto, and Zainalabedin Navabi. AFTAB: a RISC-V implementation with configurable gateways for security. In IEEE, editor, *2021 IEEE East–West Design & Test Symposium (EWDTS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Raza:2023:ODI**

[RSA+23] Muhammad Ali Raza, Iraj Shahzad, Hafsa Anwar, Muhammad Ali Qureshi, Farhan Hassan Malik, and Muhammad Usman Ali Khan. An optimum design and implementation of a 16-bit ALU on CADENCE using RISC-V architecture. In

IEEE, editor, *2023 IEEE International Conference on Emerging Trends in Engineering, Sciences and Technology (ICES&T)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Roodsari:2023:LCL**

[RSM+23] Mahboobe Sadeghipour Roodsari, Fatemeh Sheikhshoaei, Nicolo Maunero, Paolo Prinetto, and Zain Navabi. LiFi-CFI: Light-weight fine-grained hardware CFI protection for RISC-V. In IEEE, editor, *2023 IEEE International Conference on Design, Test and Technology of Integrated Systems (DTTIS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Ramirez:2020:FDR**

[RSR20] Wilmer Ramirez, Marco Sarmiento, and Elkim Roa. A flexible debugger for a RISC-V based 32-bit System-on-Chip. In IEEE, editor, *2020 IEEE 11th Latin American Symposium on Circuits & Systems (LASCAS)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**RK:2021:VBP**

[RSR21] Risikesh RK, Sharad Sinha, and Nanditha Rao. Variable bit-precision vector extension for RISC-V based processors. In IEEE, editor, *2021 IEEE 14th International Symposium on Embedded Multicore/Manycore Systems-on-Chip (MCSoC)*, pages 114–121. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Rogers:2019:SLB**

[RSRT19] Samuel Rogers, Joshua Slycord, Ronak Raheja, and Hamed Tabkhi. Scalable LLVM-based accelerator modeling in gem5. *IEEE Computer Architecture Letters*, 18(1):18–21, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

**Riedel:2021:BFL**

[RSS+21] Samuel Riedel, Fabian Schuiki, Paul Scheffler, Florian Zaruba, and Luca Benini. Banshee: a fast LLVM-based RISC-V binary translator. In IEEE, editor, *2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, pages 1–9. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Ramos:2019:APM**

[RTRM19] A. Ramos, R. G. Toral, P. Reviriego, and J. A. Maestro. An ALU protection methodology for soft processors on SRAM-based FPGAs. *IEEE Transactions on Computers*, 68(9): 1404–1410, September 2019. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Rovinski:2019:GGR**

[RZAH+19a] Austin Rovinski, Chun Zhao, Khalid Al-Hawaj, Paul Gao, Shaolin Xie, Christopher Torng, Scott Davidson, Aporva Amarnath, Luis Vega, Bandhav Veluri, Anuj Rao, Tutu Ajayi, Julian Puscar, Steve Dai, Ritchie Zhao, Dustin Richmond, Zhiru Zhang, Ian Galton, Christopher Batten, Michael B. Taylor, and Ronald G. Dreslinski. A 1.4 GHz 695 giga RISC-V inst/s 496-core manycore processor with mesh on-chip network and an all-digital synthesized PLL in 16nm CMOS. In IEEE, editor, *2019 Symposium on VLSI Circuits*, pages C30–C31. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Rovinski:2019:ECN**

[RZAH+19b] Austin Rovinski, Chun Zhao, Khalid Al-Hawaj, Paul Gao, Shaolin Xie, Christopher Torng, Scott Davidson, Aporva Amarnath, Luis Vega, Bandhav Veluri, Anuj Rao, Tutu Ajayi, Julian Puscar, Steve Dai, Ritchie Zhao, Dustin Richmond, Zhiru Zhang, Ian Galton, Christopher Batten, Michael B. Taylor, and Ronald G. Dreslinski. Evaluating Celerity: a 16-nm 695 Giga-RISC-V instructions/s manycore processor with synthesizable PLL. *IEEE Solid-State Circuits Letters*, 2(12):289–292, 2019. ISSN 2573-9603.

**Scheipel:2022:MRR**

[SAB22] Tobias Scheipel, Florian Angermair, and Marcel Baunach. moreMCU: a runtime-reconfigurable RISC-V platform for sustainable embedded systems. In IEEE, editor, *2022 25th Euromicro Conference on Digital System Design (DSD)*, pages 24–31. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Suarez:2024:CAE**

[SAB24] Daniel Suárez, Francisco Almeida, and Vicente Blanco. Comprehensive analysis of energy efficiency and performance of ARM and RISC-V SoCs. *The Journal of Supercomputing*, 80(9):

12771–12789, June 2024. CODEN JOSUED. ISSN 0920-8542 (print), 1573-0484 (electronic). URL https://link.springer.com/article/10.1007/s11227-024-05946-9.

**Sarraseca:2023:SOS**

[SAF+23] Marcel Sarraseca, Sergi Alcaide, Francisco Fuentes, Juan Carlos Rodriguez, Feng Chang, Ilham Lasfar, Ramon Canal, Francisco J. Cazorla, and Jaume Abella. SafeLS: an open source implementation of a lockstep NOEL-V RISC-V core. In IEEE, editor, *2023 IEEE 29th International Symposium on On-Line Testing and Robust System Design (IOLTS)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Sahin:2023:TCF**

[Sah23] Veysel Harun Sahin. Turna: a control flow graph reconstruction tool for RISC-V architecture. *Computing*, 105(8):1821–1845, August 2023. CODEN CMPTA2. ISSN 0010-485X (print), 1436-5057 (electronic). URL https://link.springer.com/article/10.1007/s00607-023-01172-y.

**Schmidt:2020:PFG**

[SAW+20] Colin Schmidt, Alon Amid, John Wright, Ben Keller, Howard Mao, Keertana Settaluri, Jarno Salomaa, Jerry Zhao, Albert Ou, Krste Asanović, and Borivoje Nikolić. Programmable fine-grained power management and system analysis of RISC-V vector processors in 28-nm FD-SOI. *IEEE Solid-State Circuits Letters*, 3:210–213, 2020. ISSN 2573-9603.

**Snelgrove:2023:SPT**

[SB23] Martin Snelgrove and Robert Beachler. speedAI240: a 2-petaflop, 30-Teraflops/W at-memory inference acceleration device with 1456 RISC-V cores. *IEEE Micro*, 43(3):58–63, May/June 2023. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

**Savas:2021:GHS**

[SBJ21] Süleyman Savas, Endri Bezati, and Jörn W. Janneck. Generating hardware and software for RISC-V cores generated with Rocket Chip generator. In IEEE, editor, *2021 IEEE 34th International System-on-Chip Conference (SOCC)*, pages 89–94. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Sartori:2017:GFM**

[SC17] Marcos L. L. Sartori and

Ney L. V. Calazans. Go functional model for a RISC-V asynchronous organisation — ARV. In IEEE, editor, *2017 24th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pages 381–348. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017.

**Silveira:2022:PRV**

[SCA+22] Jonathas Silveira, Lucas Castro, Victor Araújo, Rodrigo Zeli, Daniel Lazari, Marcelo Guedes, Rodolfo Azevedo, and Lucas Wanner. Prof5: a RISC-V profiler tool. In IEEE, editor, *2022 IEEE 34th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, pages 201–210. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Srivastava:2021:OSS**

[SCL+21] Abhishek Kumar Srivastava, Kirana CS, Dilip Lilaramani, Rakshitha R, and Kavya Sree. An open-source SWUpdate and Hawkbit framework for OTA updates of RISC-V based resource constrained devices. In IEEE, editor, *2021 2nd International Conference on Communication, Computing and Industry 4.0 (C2I4)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Sordillo:2021:CVA**

[SCM+21] Stefano Sordillo, Abdallah Cheikh, Antonio Mastrandrea, Francesco Menichelli, and Mauro Olivieri. Customizable vector acceleration in extreme-edge computing: a RISC-V software/hardware architecture study on VGG-16 implementation. *Electronics*, 10 (4):518–538, February 2021. ISSN 2079-9292.

**Schiavone:2017:SSW**

[SCR+17] Pasquale Davide Schiavone, Francesco Conti, Davide Rossi, Michael Gautschi, Antonio Pullini, Eric Flamand, and Luca Benini. Slow and steady wins the race? A comparison of ultra-low-power RISC-V cores for Internet-of-Things applications. In IEEE, editor, *2017 27th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017.

**Scherer:2023:SLP**

[SED+23] Moritz Scherer, Manuel Eggimann, Alfio Di Mauro, Arpan Suravi Prasad, Francesco Conti, Davide Rossi, Jorge Tomás Gómez, Ziyun Li, Syed Shakib Sarwar, Zhao Wang, Barbara De Salvo, and Luca Benini. Siracusa: a low-power on-sensor RISC-V SoC for extended reality visual processing in 16nm CMOS. In IEEE, editor, *ESSCIRC 2023- IEEE 49th European Solid State Circuits Conference (ESSCIRC)*, pages 217–220. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**SEGGER:2020:SFP**

[SEG20] SEGGER Microcontroller. SEGGER floating-point library. Web site., January 2020. URL `https://www.segger.com/products/development-tools/runtime-library/technology/floating-point-library/`.

**SRC:2019:RVM**

[SEM19] SEMICO Research Corporation. RISC-V market analysis: The new kid on the block. Web document., November 2019. URL `https://semico.com/sites/default/files/TOC_CC315-19.pdf`. Study number CC315-19.

**Sewell:2021:EFS**

[Sew21] Peter Sewell. Engineering with full-scale formal architecture: Morello, CHERI, Armv8-A, and RISC-V. In IEEE, editor, *2021 Formal Methods in Computer Aided Design (FMCAD)*, page 12. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Sanchez-Flores:2022:RCA**

[SFAAL22] Alejandra Sanchez-Flores, Lluc Alvarez, and Bartomeu Alorda-Ladaria. A review of CNN accelerators for embedded systems based on RISC-V. In IEEE, editor, *2022 IEEE International Conference on Omnilayer Intelligent Systems (COINS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Singh:2020:DIB**

[SFGB20] Aslesa Singh, Neil Franklin, Nidhi Gaur, and Paursuh Bhulania. Design and implementation of a 32-bit ISA RISC-V processor core using Virtex-7 and Virtex-UltraScale. In IEEE, editor, *2020 IEEE 5th International Conference on Computing Communication and Automation (ICCCA)*, pages 126–130. IEEE Com-

puter Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Sadrabadi:2023:ESE**

[SG23] Bahareh Ebrahimi Sadrabadi and Catherine H. Gebotys. Exploring security of embedded SRAM in PIC and RISC-V chips: Insights from image processing of low-cost photon emission microscopy. In IEEE, editor, *2023 IEEE Physical Assurance and Inspection of Electronics (PAINE)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Salazar-Garcia:2017:RVB**

[SGCGCR17] Carlos Salazar-García, Reinaldo Castro-González, and Alfonso Chacón-Rodríguez. RISC-V based sound classifier intended for acoustic surveillance in protected natural environments. In IEEE, editor, *2017 IEEE 8th Latin American Symposium on Circuits & Systems (LASCAS)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017.

**S:2023:DMC**

[SGP+23] Sajin S, Shubham Sunil Garag, Anuj Phegade, Deepshikha Gusain, and Kuruvilla Varghese. Design of a multi-core compatible Linux bootable 64-bit out-of-order RISC-V processor core. In IEEE, editor, *2023 36th International Conference on VLSI Design and 2023 22nd International Conference on Embedded Systems (VLSID)*, pages 42–47. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Stapf:2021:HWT**

[SJBS21] Emmanuel Stapf, Patrick Jauernig, Ferdinand Brasser, and Ahmad-Reza Sadeghi. In hardware we trust? From TPM to enclave computing on RISC-V. In IEEE, editor, *2021 IFIP/IEEE 29th International Conference on Very Large Scale Integration (VLSI-SoC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Selg:2023:MBO**

[SJER23] Hardi Selg, Maksim Jenihhin, Peeter Ellervee, and Jaan Raik. ML-based online design error localization for RISC-V implementations. In IEEE, editor, *2023 IEEE 29th International Symposium on On-Line Testing and Robust*

*System Design (IOLTS)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Sharma:2020:CRV**

[SJM+20] Niraj Sharma, Riya Jain, Madhumita Mohan, Sachin Patkar, Rainer Leupers, Nikhil Rishiyur, and Farhad Merchant. CLARINET: a RISC-V based framework for posit arithmetic empiricism. *arXiv.org*, ??(??):1–20, May 30, 2020. URL `https://arxiv.org/abs/2006.00364`.

**Sharma:2023:CQE**

[SJP+23] Niraj N. Sharma, Riya Jain, Mohana Madhumita Pokkuluri, Sachin B. Patkar, Rainer Leupers, Rishiyur S. Nikhil, and Farhad Merchant. CLARINET: A quire-enabled RISC-V-based framework for posit arithmetic empiricism. *Journal of Systems Architecture*, 135: 102801, 2023. CODEN JSARFB. ISSN 1383-7621 (print), 1873-6165 (electronic). URL `https://www.sciencedirect.com/science/article/pii/S1383762122002867`.

**Safari:2023:HHP**

[SJR+23] Negin Safari, Amirmahdi Joudi, Maryam Rajabalipanah, Zahra Jahanpeima, Hasan Sadeghzadeh, and Zainalabedin Navabi. HIRMA: High-performance implementation for RISC-V microcontroller applications. In IEEE, editor, *2023 IEEE East–West Design & Test Symposium (EWDTS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Song:2022:HER**

[SJYZ22] Yifan Song, Bowen Jia, Boyuan Yang, and Pei Zhang. Hummingbird E203 RISC-V processor core-based traffic flow detection system design. In IEEE, editor, *2022 IEEE International Conference on Advances in Electrical Engineering and Computer Applications (AEECA)*, pages 823–826. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Swakath:2022:DPE**

[SKK+22] S. U. Swakath, Abhijit Kshirsagar, Koteswararao Kondepu, Satish Naik Banavath, Andrii Chub, and Dmitri Vinnikov. Development of a power electronics controller with RISC-V based core for security-critical applications. In IEEE, editor, *2022 IEEE 63th International Scientific Conference on Power*

*and Electrical Engineering of Riga Technical University (RTUCON)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Soulard:2022:RVB**

[SLB+22] Guillaume Soulard, Gabriel P. Lachance, Élodie Boisselier, Mounir Boukadoum, and Amine Miled. RISC-V based processor architecture for an embedded visible light spectrophotometer. In IEEE, editor, *2022 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, pages 360–363. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Saussereau:2023:ASO**

[SLBJ23] Jonathan Saussereau, Camille Leroux, Jean-Baptiste Begueret, and Christophe Jego. AsteRISC: a size-optimized RISC-V core for design space exploration. In IEEE, editor, *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Sun:2021:LPB**

[SLCK21] Mingjian Sun, Yuan Li, Song Chen, and Yi Kang. A low power branch prediction for deep learning on RISC-V processor. In IEEE, editor, *2021 IEEE 32nd International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pages 203–206. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Santos:2021:CRV**

[SLK+21] Douglas A. Santos, Lucas M. Luza, Maria Kastriotou, Carlo Cazzaniga, Cesar A. Zeferino, Douglas R. Melo, and Luigi Dilillo. Characterization of a RISC-V System-on-Chip under neutron radiation. In IEEE, editor, *2021 16th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Swain:2021:DNS**

[SLMS21] Mahendra Swain, Dilip Lilaramani, G. Mahesh, and A. K. Srivastva. A decentralized network to secure smart grid transactions us-

ing Ethereum on RISC-V. In IEEE, editor, *2021 IEEE 2nd International Conference on Applied Electromagnetics, Signal Processing, & Communication (AESPC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Santos:2020:LCF**

[SLZ+20] Douglas Almeida Santos, Lucas Matana Luza, Cesar Albenes Zeferino, Luigi Dilillo, and Douglas Rossi Melo. A low-cost fault-tolerant RISC-V processor for space systems. In IEEE, editor, *2020 15th Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Scheipel:2017:SAP**

[SMB17] Tobias Scheipel, Fabian Mauroner, and Marcel Baunach. System-aware performance monitoring unit for RISC-V architectures. In IEEE, editor, *2017 Euromicro Conference on Digital System Design (DSD)*, pages 86–93. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017.

**Sharif:2022:CCA**

[SMGS22] Uzair Sharif, Daniel Mueller-Gritschneder, and Ulf Schlichtmann. COMPAS: Compiler-assisted software-implemented hardware fault tolerance for RISC-V. In IEEE, editor, *2022 11th Mediterranean Conference on Embedded Computing (MECO)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Smith:2024:RVA**

[Smi24] Stephen Smith. *RISC-V Assembly Language Programming: Unlock the Power of the RISC-V Instruction Set*. Maker Innovations Series. Apress, Berkeley, CA, USA, 2024. ISSN 2948-2550. xxiv + 355 pp. URL `https://link.springer.com/book/10.1007/979-8-8688-0137-2`.

**Shepherd:2021:LVL**

[SMJ21] Carlton Shepherd, Konstantinos Markantonakis, and Georges-Axel Jaloyan. LIRA-V: Lightweight remote attestation for constrained RISC-V devices. In IEEE, editor, *2021* IEEE Security and Privacy *Workshops (SPW)*, pages 221–227. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver

Spring, MD 20910, USA, 2021.

**Santos:2022:NIT**

[SML+22] Douglas A. Santos, André M. P. Mattos, Lucas M. Luza, Carlo Cazzaniga, Maria Kastriotou, Douglas R. Melo, and Luigi Dilillo. Neutron irradiation testing and analysis of a fault-tolerant RISC-V System-on-Chip. In IEEE, editor, *2022 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Santos:2023:CFT**

[SMMD23] Douglas A. Santos, André M. P. Mattos, Douglas R. Melo, and Luigi Dilillo. Characterization of a fault-tolerant RISC-V System-on-Chip for space environments. In IEEE, editor, *2023 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Stazi:2019:QAA**

[SMOM19] Giulia Stazi, Antonio Mastrandrea, Mauro Olivieri, and Francesco Menichelli. Quality aware approximate memory in RISC-V Linux kernel. In IEEE, editor, *2019 15th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, pages 177–180. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Sa:2022:FLR**

[SMP22] Bruno Sá, José Martins, and Sandro Pinto. A first look at RISC-V virtualization from an embedded systems perspective. *IEEE Transactions on Computers*, 71(9): 2177–2190, September 2022. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Sakamoto:2022:EEN**

[SNH22] Keisuke Sakamoto, Masanori Natsui, and Takahiro Hanyu. Energy-efficient nonvolatile RISC-V CPU with a custom instruction-controlled accelerator. In IEEE, editor, *2022 IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Sud:2022:ECE**

[SNK22] Parangat Sud, Shekoufeh

Neisarian, and Elif Bilge Kavun. Evaluating cryptographic extensions on a RISC-V simulation environment. In IEEE, editor, *2022 25th Euromicro Conference on Digital System Design (DSD)*, pages 548–555. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Saarinen:2022:DRV**

[SNM22] Markku-Juhani O. Saarinen, G. Richard Newell, and Ben Marshall. Development of the RISC-V entropy source interface. *Journal of Cryptographic Engineering*, 12(4):371–386, November 2022. CODEN ???? ISSN 2190-8508 (print), 2190-8516 (electronic). URL `https://link.springer.com/article/10.1007/s13389-021-00275-6`.

**Suzaki:2020:LIP**

[SNOT20] Kuniyasu Suzaki, Kenta Nakajima, Tsukasa Oi, and Akira Tsukamoto. Library implementation and performance analysis of GlobalPlatform TEE internal API for Intel SGX and RISC-V keystone. In IEEE, editor, *2020 IEEE 19th International Conference on Trust, Security and Privacy in Computing and Communications (TrustCom)*, pages 1200–1208. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Suzaki:2021:TPG**

[SNOT21] Kuniyasu Suzaki, Kenta Nakajima, Tsukasa Oi, and Akira Tsukamoto. TS-Perf: General performance measurement of trusted execution environment and rich execution environment on Intel SGX, Arm TrustZone, and RISC-V Keystone. *IEEE Access*, 9: 133520–133530, 2021. ISSN 2169-3536.

**Soria-Pardos:2022:SGO**

[SPDLP+22] Víctor Soria-Pardos, Max Doblas, Guillem López-Paradís, Gerard Candón, Narcís Rodas, Xavier Carril, Pau Fontova-Musté, Neiel Leyva, Santiago Marco-Sola, and Miquel Moretó. Sargantana: a 1 GHz+ in-order RISC-V processor with SIMD vector extensions in 22nm FD-SOI. In IEEE, editor, *2022 25th Euromicro Conference on Digital System Design (DSD)*, pages 254–261. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Shukla:2022:LOR**

[SR22] Satyam Shukla and Kailash Chandra Ray. A low-overhead re-

configurable RISC-V quad-core processor architecture for fault-tolerant applications. *IEEE Access*, 10: 44136–44146, 2022. ISSN 2169-3536.

**Schiavone:2021:AEA**

[SRD+21] Pasquale Davide Schiavone, Davide Rossi, Alfio Di Mauro, Frank K. Gürkaynak, Timothy Saxe, Mao Wang, Ket Chong Yap, and Luca Benini. Arnold: an eFPGA-augmented RISC-V SoC for flexible and low-power IoT end nodes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 29(4):677–690, 2021. CODEN IEVSE9. ISSN 1063-8210 (print), 1557-9999 (electronic).

**Shirley:2019:IFT**

[SS19] Geraldine Shirley and Fareena Saqib. Information flow tracking in RISC-V. In IEEE, editor, *2019 IEEE 16th International Conference on Smart Cities: Improving Quality of Life Using ICT & IoT and AI (HONET-ICT)*, pages 199–200. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Stangherlin:2022:DIS**

[SS22] Kleber Stangherlin and Manoj Sachdev. Design and implementation of a secure RISC-V microprocessor. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 30(11): 1705–1715, 2022. CODEN IEVSE9. ISSN 1063-8210 (print), 1557-9999 (electronic).

**Siddiqui:2019:SDF**

[SSB+19] Ali Shuja Siddiqui, Geraldine Shirley, Shreya Bendre, Girija Bhagwat, Jim Plusquellic, and Fareena Saqib. Secure design flow of FPGA based RISC-V implementation. In IEEE, editor, *2019 IEEE 4th International Verification and Security Workshop (IVSW)*, pages 37–42. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Sarihi:2022:PEO**

[SSB22] Amin Sarihi, Michael A. Schoenfelder, and Abdel-Hameed A. Badawy. Performance evaluation of an out-of-order RISC-V CPU: a SPEC INT 2017 study. In IEEE, editor, *2022 IEEE International Performance, Computing, and Communications Conference (IPCCC)*, pages 418–419. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver

Spring, MD 20910, USA, 2022.

**Serrano:2021:LPL**

[SSD+21] Ronaldo Serrano, Marco Sarmiento, Ckristian Duran, Khai-Duy Nguyen, Trong-Thuc Hoang, Koichiro Ishibashi, and Cong-Kha Pham. A low-power low-area SoC based in RISC-V processor for IoT applications. In IEEE, editor, *2021 18th International SoC Design Conference (ISOCC)*, pages 375–376. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Syafalni:2022:RVL**

[SSD+22] Infall Syafalni, Yahwista Salomo, Chyndi Oktavia Devi, Muhammad Ali Novandhika, Nana Sutisna, Rahmat Mulyawan, and Trio Adiono. RISC-V learning framework using PYNQ FPGA. In IEEE, editor, *2022 8th International Conference on Wireless and Telematics (ICWT)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Schiavone:2018:OSV**

[SSR+18] Pasquale Davide Schiavone, Ernesto Sanchez, Annachiara Ruospo, Francesco Minervini, Florian Zaruba, Germain Haugou, and Luca Benini. An open-source verification framework for open-source cores: a RISC-V case study. In IEEE, editor, *2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, pages 43–48. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Salomo:2022:ACA**

[SSS+22] Yahwista Salomo, Infall Syafalni, Nana Sutisna, Rahmat Mulyawan, and Trio Adiono. Analysis of cache associativity and replacement policy on matrix multiplication performance in RISC-V. In IEEE, editor, *2022 International Symposium on Electronics and Smart Devices (ISESD)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Su:2020:RRV**

[Su20] Charlie Hong-Men Su. The rise of RISC-V from edge to cloud. In IEEE, editor, *2020 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, page 1. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Su:2021:FAD**

[Su21] Charlie Hong-Men Su. Flexible acceleration of data processing with RISC-V DSP, vector and custom extensions. In IEEE, editor, *2021 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, page i. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Shukla:2023:EFT**

[SUAR23] Satyam Shukla, Utkarsh, Md Azam, and Kailash Chandra Ray. An efficient fault-tolerant instruction decoder for RISC-V based dual-core soft-processors. *IEEE Transactions on Circuits and Systems I: Regular Papers*, pages 1–10, 2023. ISSN 1549-8328 (print), 1558-0806 (electronic).

**Saif:2023:FIE**

[SUM23] Md. Hasanul Banna Saif, Nahin Ul Sadad, and Md. Nazrul Islam Mondal. FPGA implementation of educational RISC-V processor suitable for embedded applications. In IEEE, editor, *2023 International Conference on Electrical, Computer and Communication Engineering (ECCE)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Suvorova:2021:ADR**

[Suv21a] E. A. Suvorova. An approach for development of RISC-V based transport layer controller. In IEEE, editor, *2021 Wave Electronics and its Application in Information and Telecommunication Systems (WECONF)*, pages 1–9. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Suvorova:2021:RVB**

[Suv21b] Elena Suvorova. RISC V based reconfigurable manager for event transmission in SpaceFibre networks. In IEEE, editor, *2021 29th Conference of Open Innovations Association (FRUCT)*, pages 356–365. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Sa:2023:CRV**

[SVM+23] Bruno Sá, Luca Valente, José Martins, Davide Rossi, Luca Benini, and Sandro Pinto. CVA6 RISC-V virtualization: Architecture, microarchitecture, and design space exploration. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 31(11):1713–1726,

2023. CODEN IEVSE9. ISSN 1063-8210 (print), 1557-9999 (electronic).

**Schmidt:2021:ECR**

[SWW+21] Colin Schmidt, John Wright, Zhongkai Wang, Eric Chang, Albert Ou, Woorham Bae, Sean Huang, Anita Flynn, Brian Richards, Krste Asanović, Elad Alon, and Borivoje Nikolić. 4.3 an eight-core 1.44GHz RISC-V vector machine in 16nm FinFET. In IEEE, editor, *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, volume 64, pages 58–60. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Schmidt:2022:ECG**

[SWW+22] Colin Schmidt, John Wright, Zhongkai Wang, Eric Chang, Albert Ou, Woorham Bae, Sean Huang, Vladimir Milovanović, Anita Flynn, Brian Richards, Krste Asanović, Elad Alon, and Borivoje Nikolić. An eight-core 1.44-GHz RISC-V vector processor in 16-nm FinFET. *IEEE Journal of Solid-State Circuits*, 57(1):140–152, 2022. CODEN IJSCBC. ISSN 0018-9200 (print), 1558-173X (electronic).

**Shu:2023:HDS**

[SWWL23] Yuqiao Shu, Zhenjiang Wang, Lei Wang, and Chengzhuo Li. Hardware design of SM2 coprocessor based on RISC-V. In IEEE, editor, *2023 3rd International Symposium on Computer Technology and Information Science (ISCTIS)*, pages 1099–1104. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Schuiki:2021:SSR**

[SZHB21] Fabian Schuiki, Florian Zaruba, Torsten Hoefler, and Luca Benini. Stream semantic registers: a lightweight RISC-V ISA extension achieving full compute utilization in single-issue cores. *IEEE Transactions on Computers*, 70(2):212–227, February 2021. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Szkandera:2021:BYO**

[Szk21] Filip Szkandera. Build your own RISC-V CPU: Even home-brew processors can use hot new tech. *IEEE Spectrum*, 58(6):16–18, June 2021. CODEN IEESAM. ISSN 0018-9235 (print), 1939-9340 (electronic).

**Tulemez:2022:ICI**

[TA22] Şafak Tülemez and Deniz Turgay Altilar. Implementation

of code integrity check module for RISC-V architecture with AES. In IEEE, editor, *2022 International Conference on Theoretical and Applied Computer Science and Engineering (ICTASCE)*, pages 148–152. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Tollec:2022:EFE**

[TAC+22] Simon Tollec, Mihail Asavoae, Damien Couroussé, Karine Heydemann, and Mathieu Jan. Exploration of fault effects on formal RISC-V microarchitecture models. In IEEE, editor, *2022 Workshop on Fault Detection and Tolerance in Cryptography (FDTC)*, pages 73–83. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Truesdell:2019:NHK**

[TBK+19] Daniel S. Truesdell, Jacob Breiholz, Sumanth Kamineni, Ningxi Liu, Albert Magyar, and Benton H. Calhoun. A 6–140-nW 11 Hz–8.2-kHz DVFS RISC-V microprocessor using scalable dynamic leakage-suppression logic. *IEEE Solid-State Circuits Letters*, 2(8):57–60, 2019. ISSN 2573-9603.

**Takagi:2019:ISC**

[TBL19] Naofumi Takagi, Sylvie Boldo, and Martin Langhammer, editors. *2019 IEEE 26th Symposium on Computer Arithmetic ARITH-26 (2019), Kyoto, Japan, 10–12 June 2019*. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, June 2019. ISBN 1-72813-366-1. ISSN 1063-6889.

**Tempel:2023:MIG**

[TBLD23] Sören Tempel, Tobias Brandt, Christoph Lüth, and Rolf Drechsler. Minimally invasive generation of RISC-V instruction set simulators from formal ISA models. In IEEE, editor, *2023 Forum on Specification & Design Languages (FDL)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Tortorella:2022:RCF**

[TBR+22] Yvan Tortorella, Luca Bertaccini, Davide Rossi, Luca Benini, and Francesco Conti. RedMulE: a compact FP16 matrix-multiplication accelerator for adaptive deep learning on RISC-V-based ultra-low-power SoCs. In IEEE, editor, *2022 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages

1099–1102. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Talaki:2021:EDV**

[TBS+21] E. Bertrand Talaki, Mathieu Bouvier Des Noes, Olivier Savry, David Hely, Simone Bacles-Min, and Romain Lemaire. Exposing data value on a RISC-V based SoC. In IEEE, editor, *2021 IEEE Physical Assurance and Inspection of Electronics (PAINE)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Taheri:2022:RHL**

[TBSH22] Farhad Taheri, Siavash Bayat-Sarmadi, and Shahriar Hadayeghparast. RISC-HD: Lightweight RISC-V processor for efficient hyperdimensional computing inference. *IEEE Internet of Things Journal*, 9(23): 24030–24037, 2022. ISSN 2327-4662.

**Tsai:2023:IDM**

[TCH23] Chun-Jen Tsai, Chun Wei Chao, and Sheng-Di Hong. Integrated dynamic memory manager for a RISC-V processor. In IEEE, editor, *2023 IFIP/IEEE 31st International Conference on Very Large Scale Integration (VLSI-SoC)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Tourres:2021:ERV**

[TCL+21] Maël Tourres, Cyrille Chavet, Bertrand Le Gal, Jérémie Crenne, and Philippe Coussy. Extended RISC-V hardware architecture for future digital communication systems. In IEEE, editor, *2021 IEEE 4th 5G World Forum (5GWF)*, pages 224–229. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Tran:2023:TFP**

[TDH+23] Thai-Ha Tran, Ba-Anh Dao, Trong-Thuc Hoang, Van-Phuc Hoang, and Cong-Kha Pham. Transition factors of power consumption models for CPA attacks on cryptographic RISC-V SoC. *IEEE Transactions on Computers*, 72(9): 2689–2700, September 2023. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Thomet:2021:FFR**

[TDPD+21] Sébastien Thomet, Serge De-Paoli, Jean-Marc Daveau, Valérie Bertin, Fady Abouzeid, Philippe Roche, Fakhreddine Ghaffari, and Olivier Romain. FIRE-

CAP: Fail-reason capturing hardware module for a RISC-V based system on a chip. In IEEE, editor, *2021 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Tine:2021:VERa**

[TEYK21] Blaise Tine, Fares Elsabbagh, Krishna Yalamarthy, and Hyesoon Kim. Vortex: Extending the RISC-V ISA for GPGPU and 3D-graphics research. *arXiv.org*, ??(??):1–13, October 21, 2021. URL `https://arxiv.org/abs/2110.10857`.

**Tehrani:2020:RVE**

[TGMD20] Etienne Tehrani, Tarik Graba, Abdelmalek Si Merabet, and Jean-Luc Danger. RISC-V extension for lightweight cryptography. In IEEE, editor, *2020 23rd Euromicro Conference on Digital System Design (DSD)*, pages 222–228. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Tehrani:2021:RPP**

[TGMD21] Etienne Tehrani, Tarik Graba, Abdelmalek Si Merabet, and Jean-Luc Danger. RSM protection of the PRESENT lightweight cipher as a RISC-V extension. In IEEE, editor, *2021 24th Euromicro Conference on Digital System Design (DSD)*, pages 325–332. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Tiwari:2019:PPE**

[TGRK19] Sugandha Tiwari, Neel Gala, Chester Rebeiro, and V. Kamakoti. PERI: a posit enabled RISC-V core. *arXiv.org*, ??(??):1–14, November 2019. URL `https://arxiv.org/pdf/1908.01466.pdf`.

**Tiwari:2021:PCP**

[TGRK21] Sugandha Tiwari, Neel Gala, Chester Rebeiro, and V. Kamakoti. PERI: a configurable posit enabled RISC-V core. *ACM Transactions on Architecture and Code Optimization*, 18(3): 25:1–25:26, June 2021. CODEN ???? ISSN 1544-3566 (print), 1544-3973 (electronic). URL `https://dl.acm.org/doi/10.1145/3446210`.

**Tiwari:2023:IDI**

[TGT+23] Ankita Tiwari, Prithwijit Guha, Gaurav Trivedi, Nitesh Gupta, Navneeth

Jayaraj, and Jan Pidanic. IndiRA: Design and implementation of a pipelined RISC-V processor. In IEEE, editor, *2023 33rd International Conference Radioelektronika (RADIOELEKTRONIKA)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Tan:2022:SPS**

[TH22] Sih Pin Tan and Yung It Ho. Scalability of post-silicon test generation for multi-core RISC-V SOC validation. In IEEE, editor, *2022 IEEE 15th International Symposium on Embedded Multicore/Manycore Systems-on-Chip (MCSoC)*, pages 14–17. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Tsai:2022:ETI**

[TL22] Chun-Jen Tsai and Yi-De Lee. Embedded TCP/IP controller for a RISC-V SoC. In IEEE, editor, *2022 IFIP/IEEE 30th International Conference on Very Large Scale Integration (VLSI-SoC)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Truesdell:2022:NSP**

[TLB+22] Daniel S. Truesdell, Xinjian Liu, Jacob Breiholz, Shourya Gupta, Shuo Li, and Benton H. Calhoun. NanoWattch: a self-powered 3-nW RISC-V SoC operable from 160mV photovoltaic input with integrated temperature sensing and adaptive performance scaling. In IEEE, editor, *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, pages 210–211. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Taka:2022:IPR**

[TLS22] Endri Taka, George Lentaris, and Dimitrios Soudris. Improving the performance of RISC-V softcores on FPGA by exploiting PVT variability and DVFS. In IEEE, editor, *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1595–1599. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Tan:2016:NVC**

[TMK+16] Yong Kiam Tan, Magnus O. Myreen, Ramana Kumar, Anthony Fox, Scott Owens, and Michael Norrish. A

new verified compiler backend for CakeML. *ACM SIGPLAN Notices*, 51(9):60–73, September 2016. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

**Trippel:2017:TMMa**

[TML+17a] Caroline Trippel, Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. TriCheck: Memory model verification at the trisection of software, hardware, and ISA. *ACM SIGARCH Computer Architecture News*, 45(1):119–133, March 2017. CODEN CANED2. ISSN 0163-5964 (print), 1943-5851 (electronic).

**Trippel:2017:TMMb**

[TML+17b] Caroline Trippel, Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. TriCheck: Memory model verification at the trisection of software, hardware, and ISA. *Operating Systems Review*, 51(2):119–133, June 2017. CODEN OSRED8. ISSN 0163-5980 (print), 1943-586X (electronic).

**Trippel:2017:TMMc**

[TML+17c] Caroline Trippel, Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. TriCheck: Memory model verification at the trisection of software, hardware, and ISA. *ACM SIGPLAN Notices*, 52(4): 119–133, April 2017. CODEN SINODQ. ISSN 0362-1340 (print), 1523-2867 (print), 1558-1160 (electronic).

**Tagliavini:2019:DES**

[TMR+19] Giuseppe Tagliavini, Stefan Mach, Davide Rossi, Andrea Marongiu, and Luca Benini. Design and evaluation of SmallFloat SIMD extensions to the RISC-V ISA. In IEEE, editor, *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 654–657. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Tsuchiya:2022:ACT**

[TOYK22] Tatsuya Tsuchiya, Kanemitsu Ootsu, Takashi Yokota, and Shun Kojima. Assembly code translation from ARM64 to RISC-V. In IEEE, editor, *2022 23rd ACIS International Summer Virtual Conference on Software Engineering, Artificial Intelligence, Networking and Parallel/Distributed Computing (SNPD-Summer)*, pages 68–73. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver

Spring, MD 20910, USA, 2022.

**Tada:2020:IGS**

[TS20] Jubee Tada and Keiichi Sato. An implementation of a grid square codes generator on a RISC-V processor. In IEEE, editor, *2020 Eighth International Symposium on Computing and Networking Workshops (CANDARW)*, pages 294–297. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Torres-Sanchez:2020:DAI**

[TSABTM20] Enrique Torres-Sánchez, Jesús Alastruey-Benedé, and Enrique Torres-Moreno. Developing an AI IoT application with open software on a RISC-V SoC. In IEEE, editor, *2020 XXXV Conference on Design of Circuits and Integrated Systems (DCIS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Tine:2022:AGR**

[TSS+22] Blaise Tine, Varun Saxena, Santosh Srivatsan, Joshua R. Simpson, Fadi Alzammar, Liam Paul Cooper, Sam Jijina, Swetha Rajagoplan, Tejaswini Anand Kumar, Jeff Young, and Hyesoon Kim. Accelerating graphic rendering on programmable RISC-V GPUs. In IEEE, editor, *2022 IEEE Hot Chips 34 Symposium (HCS)*, pages 1–15. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Talpes:2023:MDT**

[TSW+23] Emil Talpes, Debjit Das Sarma, Doug Williams, Sahil Arora, Thomas Kunjan, Benjamin Floering, Ankit Jalote, Christopher Hsiong, Chandrasekhar Poorna, Vaidehi Samant, John Sicilia, Anantha Kumar Nivarti, Raghuvir Ramachandran, Tim Fischer, Ben Herzberg, Bill McGee, Ganesh Venkataramanan, and Pete Banon. The microarchitecture of DOJO, Tesla's exa-scale computer. *IEEE Micro*, 43(3):31–39, May/June 2023. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

**Takayama:2022:IPM**

[TT22] Riku Takayama and Jubee Tada. An implementation of a pattern matching accelerator on a RISC-V processor. In IEEE, editor, *2022 Tenth International Symposium on Computing and Networking Workshops (CANDARW)*, pages 273–275. IEEE Computer So-

ciety Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Tabanelli:2022:ORF**

[TTB22] Enrico Tabanelli, Giuseppe Tagliavini, and Luca Benini. Optimizing random forest-based inference on RISC-V MCUs at the extreme edge. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 41(11):4516–4526, 2022. CODEN ITCSDI. ISSN 0278-0070 (print), 1937-4151 (electronic).

**Tran:2021:RVR**

[TTDD21] Dai Duong Tran, Thi Giang Truong, Truong Giang Do, and The Duc Do. RISC-V random test generator. In IEEE, editor, *2021 15th International Conference on Advanced Computing and Applications (ACOMP)*, pages 150–155. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Tine:2021:VERb**

[TYEK21] Blaise Tine, Krishna P. Yalamarthy, Fares Elsabbagh, and Hyesoon Kim. Vortex: Extending the RISC-V ISA for GPGPU and 3D-graphics. In ACM, editor, *MICRO '21: The 54th Annual IEEE/ACM International Symposium on Microarchitecture Proceedings. October 18–22, 2021, Virtual from Athens, Greece*, pages 754–766. ACM Press, New York, NY 10036, USA, 2021. ISBN 1-4503-8557-5.

**Tang:2022:GGP**

[TZ22] Wenkai Tang and Peiyong Zhang. GPGCN: A general-purpose graph convolution neural network accelerator based on RISC-V ISA extension. *Electronics*, 11(22):3833–3854, November 2022. ISSN 2079-9292. URL `https://www.mdpi.com/2079-9292/11/22/3833`.

**Tang:2023:VRV**

[TZG+23] Shibo Tang, Jiacheng Zhu, Yifei Gao, Jing Zhou, Dejun Mu, and Wei Hu. Verifying RISC-V privilege transition integrity through symbolic execution. In IEEE, editor, *2023 IEEE 32nd Asian Test Symposium (ATS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Tan:2021:POS**

[TZPL21] Zhangxi Tan, Lin Zhang, David Patterson, and Yi Li. PicoRio: an open-source, RISC-V small-board computer to elevate the RISC-V software ecosystem. *Tsinghua Science and Tech-*

*nology*, 26(3):384–386, 2021. CODEN TSTEF7. ISSN 1007-0214 (print), 1878-7606 (electronic).

**Tang:2021:CPT**

[TZS+21] Junlong Tang, Jun Zhang, Qiang Song, Shenbo Liu, Zhiwen Yu, and Wanghui Zou. The compilation performance tests and analysis of RISC-V compilation toolchain on the SPEC CPU(R) 2017. In IEEE, editor, *2021 9th International Symposium on Next Generation Electronics (ISNE)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Uytterhoeven:2018:SPC**

[UD18] Roel Uytterhoeven and Wim Dehaene. A sub 10 pJ/Cycle over a 2 to 200 MHz performance range RISC-V microprocessor in 28 nm FDSOI. In IEEE, editor, *ESSCIRC 2018 — IEEE 44th European Solid State Circuits Conference (ESSCIRC)*, pages 236–239. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Uytterhoeven:2020:CDB**

[UD20] Roel Uytterhoeven and Wim Dehaene. Completion detection-based timing error detection and correction in a near-threshold RISC-V microprocessor in FDSOI 28 nm. *IEEE Solid-State Circuits Letters*, 3:230–233, 2020. ISSN 2573-9603.

**Mian:2019:CAE**

[uhMSI19] Riaz ul-haque Mian, Michihiro Shintani, and Michiko Inoue. Cycle-accurate evaluation of software-hardware co-design of decimal computation in RISC-V ecosystem. In IEEE, editor, *2019 32nd IEEE International System-on-Chip Conference (SOCC)*, pages 412–417. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Ushakov:2022:THM**

[USQ+22] V. Ushakov, S. Sovio, Q. Qi, V. Nayani, V. Manea, P. Ginzboorg, and J. E. Ekberg. Trusted Hart for mobile RISC-V security. In IEEE, editor, *2022 IEEE International Conference on Trust, Security and Privacy in Computing and Communications (TrustCom)*, pages 1587–1596. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Vasudev:2022:ITR**

[VKG22] Srikrishna Vasudev, Karthickraj K, and Anuj Grover.

Up to 13.7% increase in throughput of RISC V SoC using timing speculative razor SRAM. In IEEE, editor, *2022 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pages 222–225. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Vizcaino:2023:ALV**

[VMFL23] Pablo Vizcaino, Filippo Mantovani, Roger Ferrer, and Jesus Labarta. Acceleration with long vector architectures: Implementation and evaluation of the FFT kernel on NEC SX-Aurora and RISC-V vector extension. *Concurrency and Computation: Practice and Experience*, 35(20): e7424:1–e7424:??, September 10, 2023. CODEN CCPEBO. ISSN 1532-0626 (print), 1532-0634 (electronic).

**Venkateswarlu:2022:TPA**

[VMO+22] Sankatali Venkateswarlu, Subrat Mishra, Herman Oprins, Bjorn Vermeersch, Moritz Brunion, Jun-Han Han, Mircea R. Stan, Pieter Weckx, and Francky Catthoor. Thermal performance analysis of Mempool RISC-V multicore SoC. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 30(11): 1668–1676, 2022. CODEN IEVSE9. ISSN 1063-8210 (print), 1557-9999 (electronic).

**Venkateswarlu:2023:IDI**

[VMO+23] Sankatali Venkateswarlu, Subrat Mishra, Herman Oprins, Bjorn Vermeersch, Moritz Brunion, Jun-Han Han, Mircea R. Stan, Dwaipayan Biswas, Pieter Weckx, and Francky Catthoor. Impact of 3-D integration on thermal performance of RISC-V MemPool multicore SOC. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 31(12):1896–1904, 2023. CODEN IEVSE9. ISSN 1063-8210 (print), 1557-9999 (electronic).

**Vijaykumar:2022:MPO**

[VOK+22] Nandita Vijaykumar, Ataberk Olgun, Konstantinos Kanellopoulos, F. Nisa Bostanci, Hasan Hassan, Mehrshad Lotfi, Phillip B. Gibbons, and Onur Mutlu. `MetaSys`: a practical open-source metadata management system to implement and evaluate cross-layer optimizations. *ACM Transactions on Architecture and Code Optimization*, 19(2):26:1–26:29, June 2022. CODEN ???? ISSN 1544-3566 (print), 1544-3973 (electronic). URL `https://`

dl.acm.org/doi/10.1145/3505250.

**Vazquez:2022:ERV**

[VROdlT22] Daniel Vázquez, Alfonso Rodríguez, Andrés Otero, and Eduardo de la Torre. Extending RISC-V processor datapaths with multi-grain reconfigurable overlays. In IEEE, editor, *2022 37th Conference on Design of Circuits and Integrated Circuits (DCIS)*, pages 01–06. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Verma:2022:RVC**

[VSD22] Anu Verma, Priyamvada Sharma, and Bishnu Prasad Das. RISC-V core with approximate multiplier for error-tolerant applications. In IEEE, editor, *2022 25th Euromicro Conference on Digital System Design (DSD)*, pages 239–246. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Valente:2023:HVH**

[VTS+23] Luca Valente, Yvan Tortorella, Mattia Sinigaglia, Giuseppe Tagliavini, Alessandro Capotondi, Luca Benini, and Davide Rossi. HULK-V: a heterogeneous ultra-low-power Linux capable RISC-V SoC. In IEEE, editor, *2023 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Waterman:2021:RVIa**

[WA21] Andrew Waterman and Krste Asanović. *The RISC-V Instruction Set Manual. Volume I: Unprivileged ISA*. RISC-V International, ????, 2021. xvi + 220 pp. URL https://drive.google.com/file/d/1s0lZxUZaa7eV_O0_WsZzaurFLLww7ou5/view. Document Version 20211213.

**Waterman:2021:RVIb**

[WAH21] Andrew Waterman, Krste Asanović, and John Hauser. *The RISC-V Instruction Set Manual. Volume II: Privileged Architecture*. RISC-V International, ????, December 4, 2021. xii + 141 pp. URL https://drive.google.com/file/d/1EMip5dZlnypTk7pt4WWUKmtjUKTOkBqh/view. Document Version 20211203.

**Wang:2018:RTA**

[WBH+18] Angie Wang, Woorham Bae, Jaeduk Han, Stevo Bailey, Paul Rigge, Orhan Ocal, Zhongkai Wang, Kannan Ramchandran, Elad Alon, and Borivoje Nikolić. A real-time, Analog/Digital

co-designed 1.89-GHz bandwidth, 175-kHz resolution sparse spectral analysis RISC-V SoC in 16-nm FinFET. In IEEE, editor, *ESSCIRC 2018 — IEEE 44th European Solid State Circuits Conference (ESSCIRC)*, pages 322–325. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Wang:2019:RTG**

[WBH+19] Angie Wang, Woorham Bae, Jaeduk Han, Stevo Bailey, Orhan Ocal, Paul Rigge, Zhongkai Wang, Kannan Ramchandran, Elad Alon, and Borivoje Nikolić. A real-time, 1.89-GHz bandwidth, 175-kHz resolution sparse spectral analysis RISC-V SoC in 16-nm FinFET. *IEEE Journal of Solid-State Circuits*, 54(7): 1993–2008, 2019. CODEN IJSCBC. ISSN 0018-9200 (print), 1558-173X (electronic).

**Wei:2023:REI**

[WCGL23] Qian Wei, Enfang Cui, Yue Gao, and Tianzheng Li. A review of edge intelligence applications based on RISC-V. In IEEE, editor, *2023 2nd International Conference on Computing, Communication, Perception and Quantum Technology (CCPQT)*, pages 115–119. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Wu:2023:ERR**

[WCL23] Bing-Chen Wu, Wei-Ting Chen, and Tsung-Te Liu. An error-resilient RISC-V microprocessor with a fully integrated DC–DC voltage regulator for near-threshold operation in 28-nm CMOS. *IEEE Journal of Solid-State Circuits*, 58(11):3275–3285, 2023. CODEN IJSCBC. ISSN 0018-9200 (print), 1558-173X (electronic).

**Wang:2022:RSP**

[WDM22] Hui Wang, Yuyuan Du, and Xiangcheng Mu. Research on in-system programming IP of RISC-V processor. In IEEE, editor, *2022 2nd International Conference on Algorithms, High Performance Computing and Artificial Intelligence (AHPCAI)*, pages 264–269. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Wu:2023:SVR**

[WGZ+23] Lingjuan Wu, Yifei Gao, Jiacheng Zhu, Yu Tai, and Wei Hu. Security verification of RISC-V system based on ISA level information flow tracking. In IEEE, editor, *2023 IEEE*

*32nd Asian Test Symposium (ATS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Wu:2022:FIP**

[WHB+22] Zhongpan Wu, Karim Hammad, Abel Beyene, Yunus Dawji, Ebrahim Ghafar-Zadeh, and Sebastian Magierowski. An FPGA implementation of a portable DNA sequencing device based on RISC-V. In IEEE, editor, *2022 20th IEEE Interregional NEWCAS Conference (NEWCAS)*, pages 417–420. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Waterman:2013:RVI**

[WLA+13] Andrew Waterman, Yunsup Lee, Rimas Avizienis, Henry Cook, David Patterson, and Krste Asanovic. The RISC-V instruction set. In IEEE, editor, *2013 IEEE Hot Chips 25 Symposium (HCS)*, page 1. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2013.

**Wu:2022:ICH**

[WLC22] Hailong Wu, Jindong Li, and Xiang Chen. Implementation of CNN heterogeneous scheme based on domestic FPGA with RISC-V soft core CPU. In IEEE, editor, *2022 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, pages 158–159. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Wang:2023:RCA**

[WLI23] Hansen Wang, Dongju Li, and Tsuyoshi Isshiki. Reconfigurable CNN accelerator embedded in instruction extended RISC-V core. In IEEE, editor, *2023 6th International Conference on Electronics Technology (ICET)*, pages 945–954. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Wang:2021:XGA**

[WLW+21] Xi Wang, John D. Leidel, Brody Williams, Alan Ehret, Miguel Mark, Michel A. Kinsy, and Yong Chen. xBGAS: a global address space extension on RISC-V for high performance computing. In IEEE, editor, *2021 IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, pages 454–463. IEEE Computer Society Press, 1109 Spring Street, Suite 300,

Silver Spring, MD 20910, USA, 2021.

**Wang:2022:DBO**

[WLY+22] Wenzhu Wang, Xiaodong Liu, Jie Yu, Jianfeng Li, Zhou Mao, Zhuoheng Li, Chenguang Ding, and Chao Zhang. The design and building of openKylin on RISC-V architecture. In IEEE, editor, *2022 15th International Conference on Advanced Computer Theory and Engineering (ICACTE)*, pages 88–91. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Wessman:2021:RFR**

[WMA+21] Nils-Johan Wessman, Fabio Malatesta, Jan Andersson, Paco Gomez, Miguel Masmano, Vicente Nicolau, Jimmy Le Rhun, Guillem Cabo, Francisco Bas, Ruben Lorenzo, Oriol Sala, David Trilla, and Jaume Abella. De-RISC: the first RISC-V space-grade platform for safety-critical systems. In IEEE, editor, *2021 IEEE Space Computing Conference (SCC)*, pages 17–26. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Weingarten:2023:PFV**

[WMGD23] Lennart Weingarten, Alireza Mahzoon, Mehran Goli, and Rolf Drechsler. Polynomial formal verification of a processor: a RISC-V case study. In IEEE, editor, *2023 24th International Symposium on Quality Electronic Design (ISQED)*, pages 1–7. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Wessman:2022:RCR**

[WMR+22] Nils-Johan Wessman, Fabio Malatesta, Stefano Ribes, Jan Andersson, Antonio García-Vilanova, Miguel Masmano, Vicente Nicolau, Paco Gomez, Jimmy Le Rhun, Sergi Alcaide, Guillem Cabo, Francisco Bas, Pedro Benedicte, Fabio Mazzocchetti, and Jaume Abella. De-RISC: a complete RISC-V based space-grade platform. In IEEE, editor, *2022 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 802–807. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Wang:2017:LWF**

[WRD+17] Angie Wang, Brian Richards, Palmer Dabbelt, Howard Mao, Stevo Bailey, Jaeduk Han, Eric Chang, James Dunn, Elad Alon, and Borivoje Nikolić. A

0.37mm2 LTE/Wi-Fi compatible, memory-based, runtime-reconfigurable 2n3m5k FFT accelerator integrated with a RISC-V core in 16nm FinFET. In IEEE, editor, *2017 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pages 305–308. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017.

**Wistoff:2021:MTC**

[WSG+21] Nils Wistoff, Moritz Schneider, Frank K. Gürkaynak, Luca Benini, and Gernot Heiser. Microarchitectural timing channels and their prevention on an open-source 64-bit RISC-V core. In IEEE, editor, *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 627–632. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Wright:2020:DCR**

[WSK+20] John Charles Wright, Colin Schmidt, Ben Keller, Daniel Palmer, Dabbelt, Jaehwa Kwak, Vighnesh Iyer, Nandish Mehta, Pi-Feng Chiu, Stevo Bailey, Krste Asanović, and Borivoje Nikolić. A dual-core RISC-V vector processor with on-chip fine-grain power management in 28-nm FD-SOI. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 28(12):2721–2725, 2020. CODEN IEVSE9. ISSN 1063-8210 (print), 1557-9999 (electronic).

**Wali:2020:AIO**

[WSMRM20] Imran Wali, Alfonso Sánchez-Macián, Alexis Ramos, and Juan Antonio Maestro. Analyzing the impact of the operating system on the reliability of a RISC-V FPGA implementation. In IEEE, editor, *2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Werner:2019:PRV**

[WSUM19] Mario Werner, Robert Schilling, Thomas Unterluggauer, and Stefan Mangard. Protecting RISC-V processors against physical attacks. In IEEE, editor, *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1136–1141. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Wang:2019:ASM**

[WT19] Yajie Wang and Nianxiong Tan. An application-specific

microprocessor for energy metering based on RISC-V. In IEEE, editor, *2019 International Conference on IC Design and Technology (ICICDT)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Watanabe:2021:IWG**

[WTS21] Rei Watanabe, Jubee Tada, and Keiichi Sato. An implementation of a world grid square codes generator on a RISC-V processor. In IEEE, editor, *2021 Ninth International Symposium on Computing and Networking Workshops (CANDARW)*, pages 309–312. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Wu:2023:DRV**

[WTY+23] Fan Wu, Junyang Tian, Guoyan Yang, Haitao Gui, and Yuteng Luo. Design of RISC-V heterogeneous multi-core SOC architecture for edge computing for power applications. In IEEE, editor, *2023 IEEE 6th Information Technology,Networking,Electronic and Automation Control Conference (ITNEC)*, volume 6, pages 701–708. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Wang:2020:UVP**

[WTZ+20] Jiayi Wang, Nianxiong Tan, Yangfan Zhou, Ting Li, and Junhu Xia. A UVM verification platform for RISC-V SoC from module to system level. In IEEE, editor, *2020 IEEE 5th International Conference on Integrated Circuits and Microsystems (ICICM)*, pages 242–246. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Wilson:2019:NRT**

[WW19] Andrew Elbert Wilson and Michael Wirthlin. Neutron radiation testing of fault tolerant RISC-V soft processor on Xilinx SRAM-based FPGAs. In IEEE, editor, *2019 IEEE Space Computing Conference (SCC)*, pages 25–32. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Wilson:2021:FIT**

[WW21] Andrew E. Wilson and Michael Wirthlin. Fault injection of TMR open source RISC-V processors using dynamic partial reconfiguration on SRAM-based FPGAs. In IEEE, editor,

*2021 IEEE Space Computing Conference (SCC)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Wilson:2023:NRT**

[WWB23] Andrew E. Wilson, Michael Wirthlin, and Nathan G. Baker. Neutron radiation testing of RISC-V TMR soft processors on SRAM-based FPGAs. *IEEE Transactions on Nuclear Science*, 70(4): 603–610, 2023. CODEN IRNSAM. ISSN 0018-9499 (print), 1558-1578 (electronic).

**Wang:2023:DIS**

[WWGW23] Shangshou Wang, Lei Wang, Huaili Guo, and Zhengjiang Wang. Design and implementation of SM4 coprocessor based on RISC-V. In IEEE, editor, *2023 3rd International Symposium on Computer Technology and Information Science (ISCTIS)*, pages 1052–1057. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Wang:2020:RAE**

[WWL+20] X. Wang, B. Williams, J. D. Leidel, A. Ehret, M. Kinsy, and Y. Chen. Remote Atomic Extension (RAE) for scalable high performance computing. In ACM, editor, *Proceedings of the 57th ACM/IEEE Design Automation Conference (DAC), July 2020*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020. ISBN 1-4503-6725-9, 1-72812-426-3. LCCN TA174 .D458 2019. URL `https://ieeexplore.ieee.org/document/9218589`.

**Wen:2023:WCP**

[WWN23] Elliott Wen, Gerald Weber, and Suranga Nanayakkara. WasmAndroid: a cross-platform runtime for native programming languages on Android. *ACM Transactions on Embedded Computing Systems*, 22(1):4:1–4:??, January 2023. CODEN ???? ISSN 1539-9087 (print), 1558-3465 (electronic). URL `https://dl.acm.org/doi/10.1145/3530286`.

**Wang:2023:OXE**

[WWW23] Jiaolong Wang, Lei Wang, and Peixin Wang. Optimisation of x264 encoder acceleration based on RISC-V vector instructions. In IEEE, editor, *2023 3rd International Symposium on Computer Technology and Information Science (ISCTIS)*, pages 1128–1133.

IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Wang:2024:OCC**

[WWX+24] Shihang Wang, Xingbo Wang, Zhiyuan Xu, Bingzhen Chen, Chenxi Feng, Qi Wang, and Terry Tao Ye. Optimizing CNN computation using RISC-V custom instruction sets for edge platforms. *IEEE Transactions on Computers*, 73(5):1371–1384, May 2024. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Wang:2017:RFH**

[WWZL17] Yanpeng Wang, Mei Wen, Chunyuan Zhang, and Jie Lin. RVNet: a fast and high energy efficiency network packet processing system on RISC-V. In IEEE, editor, *2017 IEEE 28th International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pages 107–110. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2017.

**Wu:2022:ACR**

[WXY+22] Zheng Wu, Wuzhen Xie, Xiaoling Yi, Haitao Yang, Ruiyao Pu, Xiankui Xiong, Haidong Yao, Chixiao Chen, Jun Tao, and Fan Yang. An automated compiler for RISC-V based DNN accelerator. In IEEE, editor, *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 3097–3101. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Wang:2023:LRV**

[WY23] Peng Wang and Zhi-Bin Yu. LLVM RISC-V RV32X graphics extension support and characteristics analysis of graphics programs. *IEEE Access*, 11:67285–67297, 2023. ISSN 2169-3536.

**Wei:2021:SIC**

[WYK21] Mengmeng Wei, Guoqiang Yang, and Fanyu Kong. Software implementation and comparison of ZUC-256, SNOW-V, and AES-256 on RISC-V platform. In IEEE, editor, *2021 IEEE International Conference on Information Communication and Software Engineering (ICICSE)*, pages 56–60. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Wang:2019:OOM**

[WZW+19] Jiawei Wang, Yuejun Zhang, Pengjun Wang, Zhicun

Luan, and Liwei Li. An orthogonal obfuscation method on extend instruction sets for sequrity RISC-V circuit. In IEEE, editor, *2019 China Semiconductor Technology International Conference (CSTIC)*, pages 1–3. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Wang:2021:CIR**

[WZW+21] Shihang Wang, Jianghan Zhu, Qi Wang, Can He, and Terry Tao Ye. Customized instruction on RISC-V for Winograd-based convolution acceleration. In IEEE, editor, *2021 IEEE 32nd International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pages 65–68. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Xin:2020:VDS**

[XHY+20] Guozhu Xin, Jun Han, Tianyu Yin, Yuchao Zhou, Jianwei Yang, Xu Cheng, and Xiaoyang Zeng. VPQC: a domain-specific vector processor for post-quantum cryptography based on RISC-V architecture. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 67(8):2672–2684, 2020. ISSN 1549-8328 (print), 1558-0806 (electronic).

**Xiang:2023:RRV**

[XLZ23] Mufan Xiang, Yongjian Li, and Yongxin Zhao. RVFC: RISC-V formal in Chisel. In IEEE, editor, *2023 International Symposium of Electronics Design Automation (ISEDA)*, pages 162–167. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Xu:2022:TDH**

[XYT+22] Yinan Xu, Zihao Yu, Dan Tang, Guokai Chen, Lu Chen, Lingrui Gou, Yue Jin, Qianruo Li, Xin Li, Zuojun Li, Jiawei Lin, Tong Liu, Zhigang Liu, Jiazhan Tan, Huaqiang Wang, Huizhe Wang, Kaifan Wang, Chuanqi Zhang, Fawang Zhang, Linjuan Zhang, Zifei Zhang, Yangyang Zhao, Yaoyang Zhou, Yike Zhou, Jiangrui Zou, Ye Cai, Dandan Huan, Zusong Li, Jiye Zhao, Zihao Chen, Wei He, Qiyuan Quan, Xingwu Liu, Sa Wang, Kan Shi, Ninghui Sun, and Yungang Bao. Towards developing high performance RISC-V processors using agile methodology. In IEEE, editor, *2022 55th IEEE/ACM International Symposium on Microarchitec-*

*ture (MICRO)*, pages 1178–1199. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Xu:2023:TDH**

[XYT+23] Yinan Xu, Zihao Yu, Dan Tang, Ye Cai, Dandan Huan, Wei He, Ninghui Sun, and Yungang Bao. Toward developing high-performance RISC-V processors using agile methodology. *IEEE Micro*, 43(4): 98–106, July/August 2023. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

**Xi:2022:HRV**

[XZW+22] Yuhao Xi, Zhendong Zhang, Yuze Wang, Wen Wang, Xiaoxia Han, Weidong Wang, and Peng Liu. A heterogeneous RISC-V SoC for confidential computing and password recovery. In IEEE, editor, *2022 7th International Conference on Integrated Circuits and Microsystems (ICICM)*, pages 500–504. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Yang:2020:AAR**

[Yan20] Chia-Hsiang Yang. AI acceleration with RISC-V for edge computing. In IEEE, editor, *2020 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, page 1. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Yandrapati:2023:DIRa**

[YBR+23] Amar Babu Yandrapati, Reshma Sri Bhuma, Siva Koteswara Rao Ragineedu, Khamar Alfaz Shaik, and Bannu Gudise. Design and implementation of RISC-V based smart insulin pump. In IEEE, editor, *2023 8th International Conference on Communication and Electronics Systems (ICCES)*, pages 133–138. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Yang:2023:ATF**

[YCL+23] Chun-Chieh Yang, Yi-Ru Chen, Hui-Hsin Liao, Yuan-Ming Chang, and Jenq-Kuen Lee. Autotuning fixed-point precision with TVM on RISC-V packed SIMD extension. *ACM Transactions on Design Automation of Electronic Systems*, 28(3):33:1–33:??, May 2023. CODEN ATASFO. ISSN 1084-4309 (print), 1557-7309 (electronic). URL `https://dl.acm.org/doi/10.1145/3569939`.

**Yang:2021:ATF**

[YLC21] Dun-An Yang, Jing-Jia Liou, and Harry H. Chen. Analyzing transient faults and functional error rates of a RISC-V core: a case study. In IEEE, editor, *2021 IEEE 30th Asian Test Symposium (ATS)*, pages 133–138. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Yong:2022:SLI**

[YLT22] Kin Fei Yong, Chin Theng Lim, and Wei Khoon Teng. System level IR drop impact on chip power performance signoff for RISC-V system on chip. In IEEE, editor, *2022 17th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Yen:2023:FDR**

[YLT+23] Mao-Hsu Yen, Tzu-Feng Lin, Cheng-Hao Tsou, Yan-Wei Yu, Yih-Hsia Lin, Yuan-Fu Ku, and Chien-Ting Kao. FPGA design of RISC-V MCU collaborative industrial printer control system. In IEEE, editor, *2023 IEEE 6th International Conference on Knowledge Innovation and Invention (ICKII)*, pages 142–146. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Yandrapati:2023:DIRb**

[YNYD23] Amar Babu Yandrapati, Susanka Nilagiri, Hari Krishna Yakkanti, and Pallavi Domathoti. Design and implementation of RISC-V based pacemaker. In IEEE, editor, *2023 8th International Conference on Communication and Electronics Systems (ICCES)*, pages 123–127. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Yen:2023:VIR**

[YTL+23] Mao-Hsu Yen, Cheng-Hao Tsou, Tzu-Feng Lin, Yih-Hsia Lin, Yuan-Fu Ku, and Chien-Ting Kao. VLSI implementation of RISC-V MCU with a variable stage pipeline. In IEEE, editor, *2023 IEEE 6th International Conference on Knowledge Innovation and Invention (ICKII)*, pages 161–165. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Yilmaz:2021:DIB**

[YTÖ21] Yasin Yılmaz, Yavuz Selim Tozlu, and Berna Örs. Design and implementation of a 32-bit RISC-V core. In IEEE, editor, *2021 13th International Conference on Electrical and Electronics Engineering (ELECO)*, pages 460–464. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**You:2022:RVP**

[YWZL22] Chao-Xing You, Qi-Tong Wang, Han Zhong, and Cheng Liu. RISC-V processor-based automatic access floating-point computing accelerated dataflow co-processor. In IEEE, editor, *2022 4th International Academic Exchange Conference on Science and Technology Innovation (IAECST)*, pages 647–650. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Yin:2020:HHP**

[YXH20] Tianyu Yin, Guozhu Xin, and Jun Han. HPME: a high-performance hardware memory encryption engine based on RISC-V TEE. In IEEE, editor, *2020 IEEE 15th International Conference on Solid-State & Integrated Circuit Technology (ICSICT)*, pages 1–3. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Yildiz:2021:CAR**

[YYM21] Recep Onur Yıldız and Ayse Yilmazer-Metin. CORDIC accelerator for RISC-V. In IEEE, editor, *2021 29th Telecommunications Forum (TELFOR)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Yu:2022:CSI**

[YYP+22] Xiang Yu, Zhijie Yang, Linghui Peng, Bo Lin, Wenjing Yang, and Lei Wang. CNN specific ISA extensions based on RISC-V processors. In IEEE, editor, *2022 5th International Conference on Circuits, Systems and Simulation (ICCSS)*, pages 116–120. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Zaruba:2019:CAC**

[ZB19] Florian Zaruba and Luca Benini. The cost of application-class processing: Energy and performance analysis of a Linux-ready 1.7-GHz 64-Bit RISC-V core in 22-nm FDSOI

technology. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 27(11):2629–2640, 2019. CODEN IEVSE9. ISSN 1063-8210 (print), 1557-9999 (electronic).

**Zhu:2020:HIR**

[ZBA+20] Lingjun Zhu, Lennart Bamberg, Anthony Agnesina, Francky Catthoor, Dragomir Milojevic, Manu Komalan, Julien Ryckaert, Alberto Garcia-Ortiz, and Sung Kyu Lim. Heterogeneous 3D integration for a RISC-V system with STT-MRAM. *IEEE Computer Architecture Letters*, 19(1):51–54, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).

**Zhai:2023:MCR**

[ZBZ+23] Jianwang Zhai, Chen Bai, Binwu Zhu, Yici Cai, Qiang Zhou, and Bei Yu. McPAT-Calib: a RISC-V BOOM microarchitecture power modeling framework. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 42(1): 243–256, 2023. CODEN ITCSDI. ISSN 0278-0070 (print), 1937-4151 (electronic).

**Zuo:2023:FBM**

[ZC23] Sheng Zuo and Huan Chang. FPGA based memory security and error correction system for RISC-V processor. In IEEE, editor, *2023 3rd International Conference on Frontiers of Electronics, Information and Computation Technologies (ICFEICT)*, pages 253–259. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Zheng:2022:SRV**

[ZCH22] Tian Zheng, Gang Cai, and Zhihong Huang. A soft RISC-V processor IP with high-performance and low-resource consumption for FPGA. In IEEE, editor, *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 2538–2541. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Zhang:2023:SDD**

[ZCH+23] Bin Zhang, Ye Cai, Zhiheng He, Sen Liang, and Wei He. Structured DFT development approach for Chisel-based high performance RISC-V processors. In IEEE, editor, *2023 IEEE International Test Conference in Asia (ITC-Asia)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Zimmer:2016:RRC**

[ZCNA16] Brian Zimmer, Pi-Feng Chiu, Borivoje Nikolić, and Krste Asanović. Reprogrammable redundancy for cache Vmin reduction in a 28nm RISC-V processor. In IEEE, editor, *2016 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pages 121–124. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2016.

**Zimmer:2017:RRS**

[ZCNA17] Brian Zimmer, Pi-Feng Chiu, Borivoje Nikolić, and Krste Asanović. Reprogrammable redundancy for SRAM-based cache $V_{\min}$ reduction in a 28-nm RISC-V processor. *IEEE Journal of Solid-State Circuits*, 52(10): 2589–2600, 2017. CODEN IJSCBC. ISSN 0018-9200 (print), 1558-173X (electronic).

**Zeeb:2022:RV**

[Zee22] Bjoern Zeeb. RISC-V. Web site, June 26, 2022. URL `https://wiki.freebsd.org/riscv`.

**Zoni:2022:CEF**

[ZG22] Davide Zoni and Andrea Galimberti. Cost-effective fixed-point hardware support for RISC-V embedded systems. *Journal of Systems Architecture*, 126: 102476, 2022. CODEN JSARFB. ISSN 1383-7621 (print), 1873-6165 (electronic). URL `https://www.sciencedirect.com/science/article/pii/S1383762122000595`.

**Zhang:2022:EPE**

[ZGD22] Weiyan Zhang, Mehran Goli, and Rolf Drechsler. Early performance estimation of embedded software on RISC-V processor using linear regression. In IEEE, editor, *2022 25th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, pages 20–25. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Zhang:2023:DMC**

[ZGG23] Zheng Zhang, Bo Gao, and Min Gong. Design of the main control RISC-V processor in chiplet applications. In IEEE, editor, *2023 IEEE 5th International Conference on Civil Aviation Safety and Information Technology (ICCASIT)*, pages 1419–1424. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Zhang:2021:ARV**

[ZGL+21] Yunrui Zhang, Zichao Guo,

Jian Li, Fan Cai, and Jianyang Zhou. AnnikaCore: RISC-V architecture processor design and implementation for IoT. In IEEE, editor, *2021 IEEE 15th International Conference on Anti-counterfeiting, Security, and Identification (ASID)*, pages 200–203. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Zhang:2022:ABP**

[ZGMD22] Weiyan Zhang, Mehran Goli, Alireza Mahzoon, and Rolf Drechsler. ANN-based performance estimation of embedded software for RISC-V processors. In IEEE, editor, *2022 IEEE International Workshop on Rapid System Prototyping (RSP)*, pages 22–28. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Zhang:2022:POR**

[Zha22] Luming Zhang. The porting and optimization of RISC-V UEFI boot. In IEEE, editor, *2022 7th International Conference on Intelligent Computing and Signal Processing (ICSP)*, pages 840–843. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Zhang:2018:DRC**

[ZHC+18] Quan Zhang, Yujie Huang, Yujie Cai, Yalong Pang, and Jun Han. Design of RLWE cryptoprocessor based on vector-instruction extension with RISC-V architecture. In IEEE, editor, *2018 14th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pages 1–3. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2018.

**Zhou:2023:RVB**

[ZHL+23] Haoxiang Zhou, Haiqiao Hong, Dingbang Liu, Hang Liu, Yu Xia, Kai Li, Jun Liu, Shaobo Luo, Wei Mao, and Hao Yu. RISC-V based fully-parallel SRAM computing-in-memory accelerator with high hardware utilization and data reuse rate. In IEEE, editor, *2023 IEEE 5th International Conference on Artificial Intelligence Circuits and Systems (AICAS)*, pages 1–5. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Zhang:2022:TMT**

[ZHLR22] Jipeng Zhang, Junhao

Huang, Zhe Liu, and Sujoy Sinha Roy. Time-memory trade-offs for Saber+ on memory-constrained RISC-V platform. *IEEE Transactions on Computers*, 71(11): 2996–3007, November 2022. CODEN ITCOB4. ISSN 0018-9340 (print), 1557-9956 (electronic).

**Zhang:2022:RTI**

[ZHX+22] Zhun Zhang, Qiang Hao, Dongdong Xu, Jiqing Wang, Jinhui Ma, Jinlei Zhang, Jiakang Liu, and Xiang Wang. Real-time instruction execution monitoring with hardware-assisted security monitoring unit in RISC-V embedded systems. In IEEE, editor, *2022 8th Annual International Conference on Network and Information Systems for Computers (ICNISC)*, pages 192–196. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Zhou:2020:RVG**

[ZJX20] Yuzhi Zhou, Xi Jin, and Tian Xiang. RISC-V graphics rendering instruction set extensions for embedded AI chips implementation. In ACM, editor, *SBDAI '20: 2020 2nd International Conference on Big Data and Artificial Intelligence, Johannesburg, South Africa, April 28–30, 2020*, pages 85–88. ACM Press, New York, NY 10036, USA, 2020. ISBN 1-4503-7645-2. URL `https://dl.acm.org/doi/pdf/10.1145/3378904.3378926`.

**Zhao:2023:ERV**

[ZKS+23] Yifan Zhao, Honglin Kuang, Yi Sun, Zhen Yang, Chen Chen, Jianyi Meng, and Jun Han. Enhancing RISC-V vector extension for efficient application of post-quantum cryptography. In IEEE, editor, *2023 IEEE 34th International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pages 10–17. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Zang:2019:RRV**

[ZLC19] Zhenya Zang, Yao Liu, and Ray C. C. Cheung. Reconfigurable RISC-V secure processor and SoC integration. In IEEE, editor, *2019 IEEE International Conference on Industrial Technology (ICIT)*, pages 827–832. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Zimmer:2015:RVV**

[ZLP+15] Brian Zimmer, Yunsup Lee, Alberto Puggelli,

Jaehwa Kwak, Ruzica Jevtic, Ben Keller, Stevo Bailey, Milovan Blagojevic, Pi-Feng Chiu, Hanh-Phuc Le, Po-Hung Chen, Nicholas Sutardja, Rimas Avizienis, Andrew Waterman, Brian Richards, Philippe Flatresse, Elad Alon, Krste Asanović, and Borivoje Nikolić. A RISC-V vector processor with tightly-integrated switched-capacitor DC-DC converters in 28nm FDSOI. In IEEE, editor, *2015 Symposium on VLSI Circuits (VLSI Circuits)*, pages C316–C317. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2015.

**Zimmer:2016:RVV**

[ZLP+16] Brian Zimmer, Yunsup Lee, Alberto Puggelli, Jaehwa Kwak, Ruzica Jevtić, Ben Keller, Steven Bailey, Milovan Blagojević, Pi-Feng Chiu, Hanh-Phuc Le, Po-Hung Chen, Nicholas Sutardja, Rimas Avizienis, Andrew Waterman, Brian Richards, Philippe Flatresse, Elad Alon, Krste Asanović, and Borivoje Nikolić. A RISC-V vector processor with simultaneous-switching switched-capacitor DC–DC converters in 28 nm FDSOI. *IEEE Journal of Solid-State Circuits*, 51(4): 930–942, 2016. CODEN IJSCBC. ISSN 0018-9200 (print), 1558-173X (electronic).

**Zulberti:2021:SBC**

[ZNF21] Luca Zulberti, Pietro Nannipieri, and Luca Fanucci. A script-based cycle-true verification framework to speed-up hardware and software co-design of System-on-Chip exploiting RISC-V architecture. In IEEE, editor, *2021 16th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*, pages 1–6. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Zou:2023:ABR**

[ZPL+23] Xiaofeng Zou, Yuanxi Peng, Tuo Li, Lingjun Kong, Zhaochun Pang, and Lu Zhang. Accelerating Blake3 in RISC-V. In IEEE, editor, *2023 2nd International Conference on Computing, Communication, Perception and Quantum Technology (CCPQT)*, pages 296–301. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Zgheib:2021:ERV**

[ZPRD21] Anthony Zgheib, Olivier Potin, Jean-Baptiste Rigaud, and Jean-Max Dutertre. Extending a RISC-V core with an AES hardware accelerator to meet IOT constraints. In IEEE, editor, *SMACD /PRIME 2021; International Conference on SMACD and 16th Conference on PRIME*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Zgheib:2022:CVS**

[ZPRD22] Anthony Zgheib, Olivier Potin, Jean-Baptiste Rigaud, and Jean-Max Dutertre. A CFI verification system based on the RISC-V instruction trace encoder. In IEEE, editor, *2022 25th Euromicro Conference on Digital System Design (DSD)*, pages 456–463. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Zgheib:2023:CCI**

[ZPRD23] Anthony Zgheib, Olivier Potin, Jean-Baptiste Rigaud, and Jean-Max Dutertre. CIFER: Code integrity and control flow verification for programs executed on a RISC-V core. In IEEE, editor, *2023 IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, pages 100–110. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Zhong:2023:RVB**

[ZS23] Xinchao Zhong and Chiu-Wing Sham. A RISC-V based SoC with configurable CPK sensor interface for ECU on motorcycle. In IEEE, editor, *2023 IEEE 12th Global Conference on Consumer Electronics (GCCE)*, pages 321–322. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2023.

**Zaruba:2020:CRV**

[ZSB20] Florian Zaruba, Fabian Schuiki, and Luca Benini. A 4096-core RISC-V chiplet architecture for ultra-efficient floating-point computing. In IEEE, editor, *2020 IEEE Hot Chips 32 Symposium (HCS)*, pages 1–24. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Zaruba:2021:MCR**

[ZSB21] Florian Zaruba, Fabian Schuiki, and Luca Benini. Manticore: a 4096-core RISC-V chiplet architecture

for ultraefficient floating-point computing. *IEEE Micro*, 41(2):36–42, March/April 2021. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

**Zhong:2020:RVS**

[ZSM20] Xinchao Zhong, Chiu-Wing Sham, and Longyu Ma. A RISC-V SoC for mobile payment based on visible light communication. In IEEE, editor, *2020 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pages 102–105. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Zhong:2021:HIR**

[ZSM21] Xinchao Zhong, Chiu-Wing Sham, and Longyu Ma. A highly integrated RISC-V based SoC for on-board unit in ETC system. In IEEE, editor, *2021 IEEE 10th Global Conference on Consumer Electronics (GCCE)*, pages 302–303. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Zekany:2021:TOP**

[ZTC21] Stephen A. Zekany, Jielun Tan, and James A. Connolly. Teaching out-of-order processor design with the RISC-V ISA. In IEEE, editor, *2021 ACM/IEEE Workshop on Computer Architecture Education (WCAE)*, pages 1–8. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Zhao:2023:NTF**

[ZUSK23] Yuankang Zhao, Salim Ullah, Siva Satyendra Sahoo, and Akash Kumar. NvMISC: Toward an FPGA-based emulation platform for RISC-V and nonvolatile memories. *IEEE Embedded Systems Letters*, 15(4):170–173, 2023. ISSN 1943-0663 (print), 1943-0671 (electronic).

**Zhang:2019:CBB**

[ZWB19] S. Zhang, A. Wright, and T. Bourgeat. Composable building blocks to open up processor design. *IEEE Micro*, 39(3):47–55, May/June 2019. CODEN IEMIDZ. ISSN 0272-1732 (print), 1937-4143 (electronic).

**Zhang:2020:ULP**

[ZWL+20] Yong-Liang Zhang, Wei-Zhen Wang, Qiang Li, Zhi-Yan Jia, Jun Han, Xiao-Yang Zeng, and Xu Cheng. An ultra-low-power high-precision dynamic gesture recognition coprocessor based on RISC-V architecture. In IEEE, editor, *2020*

*IEEE 15th International Conference on Solid-State & Integrated Circuit Technology (ICSICT)*, pages 1–4. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2020.

**Zheng:2023:HSC**

[ZWL+23] Xin Zheng, Junwei Wu, Xian Lin, Huaien Gao, Suting Cai, and Xiaoming Xiong. Hardware/software co-design of cryptographic SoC based on RISC-V virtual prototype. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 70(9):3624–3628, 2023. ISSN 1549-7747 (print), 1558-3791 (electronic).

**Zhao:2022:HPD**

[ZXXH22] Yifan Zhao, Ruiqi Xie, Guozhu Xin, and Jun Han. A high-performance domain-specific processor with matrix extension of RISC-V for Module-LWE applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 69 (7):2871–2884, 2022. ISSN 1549-8328 (print), 1558-0806 (electronic).

**Zhang:2020:MRB**

[ZZB+20] Jialiang Zhang, Yue Zha, Nicholas Beckwith, Bangya Liu, and Jing Li. MEG: a RISCV-based system emulation infrastructure for near-data processing using FPGAs and high-bandwidth memory. *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 13(4):19:1–19:24, October 2020. CODEN ???? ISSN 1936-7406 (print), 1936-7414 (electronic). URL `https://dl.acm.org/doi/10.1145/3409114`.

**Zhang:2021:CAE**

[ZZG21] Li Zhang, Xian Zhou, and Chuliang Guo. A CNN accelerator with embedded RISC-V controllers. In IEEE, editor, *2021 China Semiconductor Technology International Conference (CSTIC)*, pages 1–3. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Zuo:2022:HBR**

[ZZL+22] Sheng Zuo, Junjie Zhuang, Yao Liu, Mingyu Wang, and Zhiyi Yu. Hardware based RISC-V instruction set randomization. In IEEE, editor, *2022 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, pages 96–97. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2022.

**Zheng:2021:DIA**

[ZZQ21] Zhenhong Zheng, Xiangyu Zhu, and Hui Qian. Design and implementation of arbitrary point FFT based on RISC-V SoC. In IEEE, editor, *2021 IEEE 5th Advanced Information Technology, Electronic and Automation Control Conference (IAEAC)*, pages 1216–1219. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Zhang:2019:RVB**

[ZZW+19] Guohe Zhang, Kepeng Zhao, Bin Wu, Yiqun Sun, Li Sun, and Feng Liang. A RISC-V based hardware accelerator designed for Yolo object detection system. In IEEE, editor, *2019 IEEE International Conference of Intelligent Applied Systems on Engineering (ICIASE)*, pages 9–11. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2019.

**Zhang:2021:DVT**

[ZZZ21] Wendi Zhang, Yonghui Zhang, and Kun Zhao. Design and verification of three-stage pipeline CPU based on RISC-V architecture. In IEEE, editor, *2021 5th Asian Conference on Artificial Intelligence Technology (ACAIT)*, pages 697–703. IEEE Computer Society Press, 1109 Spring Street, Suite 300, Silver Spring, MD 20910, USA, 2021.

**Zhang:2023:ESH**

[ZZZ+23] Chengbo Zhang, Peiyong Zhang, Shengrui Zheng, Zhao Yang, Rui Liu, and Kaitian Huang. An efficient self-healing architecture for improving the RAS characteristics of RISC-V server and its quantitative evaluation method. *IEEE Embedded Systems Letters*, 15(1):41–44, 2023. ISSN 1943-0663 (print), 1943-0671 (electronic).