

A Complete Bibliography of Publications in *IEEE Computer Architecture Letters*

Nelson H. F. Beebe
University of Utah
Department of Mathematics, 110 LCB
155 S 1400 E RM 233
Salt Lake City, UT 84112-0090
USA

Tel: +1 801 581 5254
FAX: +1 801 581 4148

E-mail: beebe@math.utah.edu, beebe@acm.org,
beebe@computer.org (Internet)
WWW URL: <https://www.math.utah.edu/~beebe/>

24 August 2024
Version 1.11

Title word cross-reference

[JLA16, NK22, YQL+24]. **Accelerated** [FFAMK15, JLKK23, KLR24, LZL+20].
Accelerating [CPK+23, KKJ+22, KHS+24b, SK21, SPHS22, SAA+23, VRS18, WMZY17, ZZW+22]. **Acceleration** [GKK+22, HCK+21, JLRA18, KKL+15, LYY+21, LYL+16, LHZ19, RMM24, WKE12, YCH24]. **Accelerator** [BHY+19, CMP+14, DXSS15, GMPMC+23, GIH+24, KDS22, LAC14, LBB+19, LWM20, LAM+22, LHWB10, LWB13, MMY+14, NBH13, PPA+24, RSRT19, VRFT24, XHG+19, YHM17, YG18, ZL18a].
accelerator-based [LHWB10].
Accelerator-Rich [LBB+19].
Accelerators [AW15, BSMB23, FSO+22, JKK+21, KPPK21, MNFI20, MMAAK21, OSH16, PGC22, RSO21, WLDN19, YSL+21].

3 [RMMLK16, ZBA+20]. $O(1)$ [LX08].
-D [RMMLK16].
128-Bit [DPP23].
2.0 [LTB+24, PZX15]. **2.5D** [CWK+22].
3D [HRF+11, HLR21, RMM24, XYMY16].
3D-Stacked [RMM24].
4T [JDK+02].
Abstract [BEA+13]. **Abstractions** [QYZ+24]. **accel** [VRFT24]. **Accelerate**

Access [Ano13h, Ano13i, CYAW20, DSVK12, KSB19, LGLK17, MSI18, PJ22, SCR⁺17, WTSW21, XYMY16, YQL⁺24].
Access-Control [LGLK17]. **accesses** [Zha06]. **Accounting** [LJM⁺14, LMC⁺09].
Accumulate [GG17, JPC18]. **Accuracy** [DKD07, SHK15]. **Accurate** [BREM08, CAPS09, CVF⁺24, JC17, KHB⁺19, LYR⁺20, RCBJ11, SJ22]. **ACE** [BREM08]. **Achieve** [WZLQ15]. **Achieving** [NB24, SCR⁺17, WCZ⁺12]. **Across** [WXZ⁺21]. **Active** [BDJ06]. **Ad** [Ano09a].
Adapting [MNFI20]. **Adaptive** [GF16, KK21, LZLX15, MCKW10, SK21, SDTG04, SCF04, XYZ15, XYMY16, YKP⁺22, ZWL15]. **Address** [IKW⁺20, KNGK15, KJS⁺19, MKP⁺24, SfCL03, VD02, YWG17, AD06, LLLM06].
Addressable [VHN15, Yav24]. **Addressing** [ÇE14, MVJ17]. **ADL** [BVL09]. **Adopting** [LLLM06]. **ADT** [MDK⁺23]. **Advance** [KMJ18]. **Advanced** [Ano16k, KYW⁺24].
Advancing [RAD⁺23]. **Advertisement** [Ano09b, Ano09c, Ano09d, Ano09e, Ano09f, Ano09g, Ano10c, Ano10d, Ano10b, Ano10f, Ano10e, Ano12c, Ano12k, Ano10g, Ano14f].
Affinity [HLH16]. **Against** [LEBM20, ZNTJE23, OKS⁺15, SKS⁺15].
Aggregation [QYZ⁺24]. **Aggressive** [JTG23, MDK⁺23]. **Aging** [SRH20].
Aging-Aware [SRH20]. **AI** [MGH⁺22, SJS24]. **Algebraic** [GMPMC⁺23]. **Algorithm** [LX08, LAS22, XL07, YCH24].
Algorithm/Hardware [LAS22]. **Algorithms** [CLCG14]. **Aligner** [ZZJ18].
Alignment [HKO⁺22, KHS⁺24a, VRS18, ZZJ18].
Alleviating [ZZW⁺23]. **Allocation** [LLJK23, LLM⁺21, MJBD11, NPS21, PKKK23, ZWL15]. **Allocator** [KKLL22, LMK06]. **Alternative** [ÇTNL16, HBL⁺10, KZL18, MAHK18].
Amdahl [CM08, VMS17]. **Amoeba** [MPA⁺18]. **AMX** [KYW⁺24]. **Analysis** [Ano14c, Ano14d, BY17, BREM08, CNHH15, GGS19, HLH16, HLR21, KCPG18, KKP⁺18, SRS11, TOIS17, VP16].
Analytical [KZL18, SGBE18]. **Analytics** [Ano16k, HLR21, KKL20, LZL⁺20].
Analyzing [NGS15, SQ23]. **Annealers** [AQ24]. **Annual** [Ano11a, Ano12a, Ano13a].
Application [CNHH15, CV15, GSG⁺17, WCC14, ZCG18].
Application-Level [ZCG18].
Application-Specific [WCC14].
Applications [BGZT22, DVAE18, DSVK12, HMCP16, JLA16, KHS⁺24b, KPEC10, LPK16, MHM⁺24, MLK15, MKD⁺23, MGI14, MSE⁺17, ODKK18, SAA⁺23, VP16, WJA⁺19, WLL⁺22]. **Approach** [BGZT22, CV15, EGWM14, GMM⁺19, HBW⁺23, KZL18, LEBM20, PGC22, SBVB17].
Approaches [NGS15]. **Approximate** [LHPR23, SJS24]. **Approximation** [CKZ⁺20, KQD18, SRLM20]. **Arbiter** [ZAK⁺17]. **ARCE** [RADZ19].
Architecting [SYC14, ZLS10].
Architectural [GD18, HPS23, KNQ15, MKP⁺24, QYZ⁺24, SMY15, Wu14, ZLM⁺20, ZWT22].
Architecture [AWD⁺18, Ano14a, Ano14b, Ano15b, Ano15d, Ano15c, Ano15e, Ano15a, Ano16a, Ano16b, Ano17, Ano18, Ano19, Ano20, Ano21, Ano22, ACG⁺07, BDBS⁺08, BVL09, DS09, DL20, DM06, Eec22, FFAMK15, Gau09, Jac16a, JPC18, JP13, KWL13, KLS11, KLKK14, KL02, KR18, LCHL20, LKA15, LCW⁺24, LYL⁺16, LJ18, LQYF23, MMR17, OKS⁺15, PLL08, RADZ19, SRV⁺19, SRS20, SKS⁺15, SHK15, Ska13, SCR⁺17, SJA⁺17, SHJW21, SCB⁺20, SM18, TS24, VRFT24, WLL⁺22, YNS⁺08, YKP⁺22, ZL18b, ZTRA22, ZZJ18, AD06].
Architecture-Assisted [RADZ19].
Architectures [AFG⁺24, BRUS21, DXSS15, EOA⁺23, IXS18, KFJ⁺03, LLKS12, MTM18, NBH13,

RAD⁺23, RB14, SGBE18, SRT12, WCZ⁺12, WLL17, XYMY16, XGH⁺22, XWG⁺14]. **Area** [FBN⁺24, OKS⁺15, SKS⁺15, TS24]. **Area-Efficient** [OKS⁺15, SKS⁺15]. **Argumented** [YCH24]. **Argus** [NS15]. **Argus-G** [NS15]. **Array** [AS18, CTL⁺20, KLCA21, LKKS15, LWM20, WLZZ23]. **Arrays** [APK⁺18, SHW19]. **ARSENAL** [SM18]. **Assertions** [ZB19]. **Assess** [Eec22]. **Assignment** [EOA⁺23]. **Assisted** [CST⁺04, CKA20, DV13, KKL⁺23, MPPS17, PPG⁺17, RADZ19]. **Associate** [Eec13, Mar13a]. **Associative** [HCM10, KZL18, YKMG15]. **Asymmetric** [AA19, LBB⁺19, MNU⁺15, SCR⁺17, MWK⁺06]. **Atomic** [KLZ12]. **atomicity** [BLM06]. **Attached** [BSMB23]. **Attack** [ASSK21, KYP21, MLC24, MPA⁺18]. **Attacks** [BBZ⁺19, SQ23]. **Attention** [LHPR23, YQL⁺24]. **Authors** [Ano14b, Ano14d, Ano15d, Ano15e, Ano08d, Ano09n, Ano09o, Ano10o, Ano10p]. **Auto** [CXS18]. **Auto-Tuning** [CXS18]. **Automata** [AS18, AWD⁺18, SRV⁺19]. **Automata-Processing** [AWD⁺18]. **Automated** [WLN22]. **Automatic** [BVL09, LCW⁺16, YSL⁺21]. **Automatically** [MHM⁺24]. **Autonomous** [APK⁺21, KWB⁺20, MPA⁺18]. **Available** [KL18]. **AVFs** [BREM08]. **Aware** [AGJ18, APK⁺21, AS14, CCWY17, DL20, EGWM14, FPA⁺21, HCM10, JEAG⁺19, JLS⁺23, KPCK20, KQGS16, KKKH18, LZS⁺08, LA16, LQYF23, MLC24, MNU⁺15, Mus09, NPS21, PBO⁺15, SSVS21, SRH20, UKM02, Vol21, YC15, ZTS16, ZKF⁺18, ZLAE17, IPS14]. **Away** [GBK⁺09]. **AYUSH** [MV15].

B [PGJ12]. **B-Fetch** [PGJ12]. **Back** [Ano12j, Ano16p, Ano12d, Ano12e, Ano13c, Ano13d, Ano16c]. **Backend** [PDGV16]. **Backup** [MPA⁺18]. **Bad** [MCM13]. **Balanced** [Ant09, FSO⁺22, GVG⁺08, SDTG04, Zha06]. **Balancing** [ILXY18a, ZNTJE23]. **Bandwidth** [AMW15, KL18, MA19, UTT⁺24]. **Bank** [RMA⁺20, XGH⁺22]. **Banked** [RMA⁺20]. **Baobab** [TWI⁺24]. **Barrier** [CKZ⁺20]. **Basecalling** [LJ18]. **Basecalling-in-Memory** [LJ18]. **Based** [APK⁺18, BVL09, CNHH15, CPK⁺23, DC18, FD08, FBN⁺24, GLH⁺20, Hos18, IKW⁺20, JY24, KP21, KWL⁺17, KL18, KJS⁺19, KJK21, KKJ⁺22, KL02, KNE⁺14, LLKS12, LLSA18, LSJ⁺19, LCKA23, LZLX15, LHZ19, LJ18, MPPS17, MM03, MAT17, Mus09, NSC20, NGS15, PJ22, PL10, RSRT19, SSVS21, SBVB17, SJS24, SKTC05, SJM17, SRH20, SRLM20, VGMSLN⁺18, Yav24, ZZW⁺22, LAC14, LLLM06, LMK06, LHWB10, yPSS⁺10, SYC14, HH22, MGH⁺22, ZTRA22]. **Batched** [CPK⁺23]. **Bayesian** [BHY⁺19, KDL23, LLM⁺21, NR21]. **BayesTuner** [NR21]. **BDDs** [PV06]. **Be** [TLG⁺11]. **Behavior** [TV02]. **Benchmark** [ILG10, KL02, WLL17]. **Benchmarking** [MTM18, XHG⁺19, ZWT22]. **BENoC** [WCK08]. **Best** [SKTC05]. **Better** [MCM13, YSL⁺21]. **Better-Than-Bad** [MCM13]. **Between** [HSUS11, ILXY18b]. **Beyond** [Ant09, GVG⁺08]. **Bias** [KK21, RZ06]. **Bidirectional** [LYY⁺21]. **Big** [AG17, Ano16k, Jac16a, JLA16, MSE⁺17]. **Big-Data** [MSE⁺17]. **BigData** [LCHL20]. **Bin** [WLWZ19]. **Binary** [LAM⁺22]. **Birkhoff** [DC18]. **Bit** [DPP23, ILXY18a, JAM17, WSVS22]. **Bit-Level** [ILXY18a]. **Bit-Serial** [JAM17, WSVS22]. **Bitcoin** [JLKK23]. **Bitstream** [KDL23]. **Bitwise** [SHB⁺15]. **Block** [CCWY17, Jac16b, KG10, RB14, TMSA16, VD02, ZM07]. **Block-** [VD02]. **Blockchain** [JLKK23]. **Blocks** [MCM13]. **Board** [Ano08a, Ano09h, Ano09i, Ano10h,

Ano10i, Ano14a, Ano14c, Ano15b, Ano15c]. **Boomerang** [FHL⁺10]. **Boost** [VMS17]. **Bootstrapping** [KH18]. **Bottleneck** [AMW15, GGS19, KKP⁺18, LLD⁺18]. **Bottlenecks** [BHL⁺18]. **Bound** [SCL13]. **Bounded** [RSO21]. **Bounds** [SD04]. **Branch** [CSSU20, EHdSH20, GAH⁺23, MHAD15, PGJ12, ST20, SYC07]. **BRAWL** [LJ18]. **Breaking** [EHdSH20, LLD⁺18, SQ23]. **Browser** [ZWT22]. **Browsing** [ZSLR14]. **Brutus** [BGS⁺20]. **BTB** [AGK21]. **BTB-X** [AGK21]. **Buffer** [ASSK21, KLCA21, SD04, SRLP09]. **Bufferless** [DPC16, KKK13]. **Buffers** [LMJ12]. **Building** [Jac16b, MKD⁺23, ZM07]. **Bulk** [SHB⁺15]. **Bursty** [HMCP16]. **Bus** [WCK08]. **Bus-Enhanced** [WCK08]. **Butterfly** [KBD07]. **BWM** [VRS18]. **By-Software** [GAH⁺23]. **Byte** [VHN15]. **Byte-Addressable** [VHN15].

C [ZAK⁺17]. **C-State** [ZAK⁺17]. **Cabinet** [Jac16a]. **Cache** [ALKSA19, AS14, BHL⁺18, BS17, BGS⁺20, BGP⁺17, BSMB23, CWK⁺22, CCWY17, CZYY11, FJ08, GRCV02, GKKW07, IPS14, JTG23, JP13, KLS11, KG10, LLJK23, LKP⁺23, MPPS17, MA19, MCY⁺12, MCRV07, MKMJ23, NPBS23, OKS⁺15, PPG11, SSSM18, SKS⁺15, TV02, VGMSLN⁺18, VMP⁺16, WZLQ15, WKE12, XYMY16, YMG14, YFPF14, ZVYW03, ZLAE17, ZWL15, EPS06, Zha06]. **Cache-Attached** [BSMB23]. **Cache-aware** [IPS14]. **Caches** [BLKSA17, BS17, FJ08, JP13, KYP21, LKKS15, MV15, PHBC18, SSVS21, SLKD14, WMJM23, YSL⁺21, ZS18, Zha06]. **Caching** [YJZ15]. **Calculus** [BS17]. **call** [LLLM06]. **CAM** [WSVS22]. **Can** [TLG⁺11]. **Capable** [LYR⁺20]. **Capacity** [HCK22, SMLS15]. **Capsule** [HA24].

CARB [ZAK⁺17]. **Carlo** [SCL06]. **Case** [AA19, AS14, EE14, HBL⁺10, Jac16b, KK21, KWL⁺17, KKLL22, KR18, NMS14, Per21, PV06, ST20, SRT12, SKS⁺24, SCL13, Vol21, CMLV03, TD02, Zho06]. **CasHMC** [JC17]. **CAT** [LLJK23]. **CAVA** [CST⁺04]. **CEASER** [BGS⁺20]. **Celebrates** [Ano10b]. **Cells** [JDK⁺02]. **Cellular** [AS18, CTL⁺20]. **Center** [KPKK20]. **Centralized** [MCKW10]. **Centric** [HEDH21, KR18]. **CF** [CXS18]. **CF-TUNE** [CXS18]. **Chaining** [KLCA21, MJBD11]. **Chains** [AQ24]. **Challenge** [DK13]. **Challenges** [LG20, RCK21]. **Chameleon** [YNS⁺08]. **Change** [Jun17, KJS⁺19, KMJ18, Sez10]. **Channel** [MLC24]. **Channels** [KWKK18, MKMJ23, NAG17]. **Chaotic** [TS24]. **Characteristics** [NBW⁺23, ZSLR14]. **Characterization** [DS09, HS04, HLR21, SMY15, WXZ⁺21, WLL⁺22]. **Characterizing** [BKA⁺09, HXL⁺22, JSLW20, WYY⁺23, YCD⁺20, ZYZ⁺22]. **Checkpoint** [CST⁺04]. **Checkpoint-Assisted** [CST⁺04]. **Checkpointing** [MAT17]. **Chief** [Eec13, Gau09, Mar13a, Ska10a, Ska11a, Ska13]. **Chip** [AGJ18, CGY⁺14, DOM⁺07, DOM⁺08, GQLZ19, GGM⁺16, GFAHSA24, GKKW07, HCM10, KBD07, KKK13, KDS22, KLZ12, LGLK17, LZS⁺08, LMJ12, MJBD11, MTT12, PL15, PPG11, RMMLK16, SD02, WCK08, XL07, ZM07, ZNTJE23, ZZW⁺23, ZKW12, MWK⁺06, Zho06]. **Chip-Multiprocessor** [PPG11]. **Chipkill** [JSDK13]. **Chiplet** [CWK⁺22]. **Chopping** [RSO21]. **CIDR** [OKS⁺15, SKS⁺15]. **CIM** [KKL⁺07]. **Circuit** [JLP07, XJ09]. **Circuit-level** [XJ09]. **Circuit-Switched** [JLP07]. **Circuits** [EOA⁺23, ZB19]. **Claims** [BGS⁺20]. **Class** [KWKK18]. **Classification** [MLC24, SRH20]. **Classifications** [KKL⁺07]. **Client** [MLK15]. **Clock** [Mic20]. **Closing** [ILXY18b]. **Cloud**

[DK16, GD18, HLR21, LAX⁺20, PGR⁺23, WLL17]. **Clumsy** [KKK13]. **Cluster** [DRGA12, MWK⁺06]. **Clustering** [CVF⁺24, SBQK21]. **CMA** [ZL18a]. **CMP** [Jac16b, KG10, LMC⁺09, WCK08]. **CMPs** [MA19]. **CNN** [JLRA18, LWM20, SPHS22]. **CNNs** [WTSW21]. **Co** [DCG12, KWB⁺20, LAS22]. **Co-Design** [KWB⁺20]. **Co-designed** [DCG12]. **Co-Optimization** [LAS22]. **Coarse** [LYL⁺16, ZM07]. **Coarse-Grain** [ZM07]. **Coarse-Grained** [LYL⁺16]. **Code** [ALKSA19, GMMC15, KKL⁺23, RADZ19]. **Code-Pointer** [KKL⁺23]. **Codesigned** [MKM17]. **Coding** [CF24, YFPF14]. **Cognitive** [WL16]. **Coherence** [BGP⁺17, BSMB23, CWK⁺22, JLP07, KLS11, SLC03, EPS06]. **Coherency** [BHY⁺19, MAHK18]. **Coherent** [MAHK18]. **Collaborative** [ACG⁺07, CXS18]. **Collabratec** [Ano16l, Ano16m]. **collection** [Ano12k]. **Collective** [RASW19]. **Combinators** [AYL22]. **Combining** [VD02]. **Command** [GLH⁺20]. **Commands** [NBW⁺23]. **Comment** [Ant09]. **Commercial** [GIH⁺24]. **Commit** [DV13]. **Commodity** [JY24, TMNK19, Yav24]. **Communication** [BDJ06, GGM⁺16, SPAP10, TASA13, YQL⁺24, LLLM06]. **Communications** [FJ08, RASW19]. **Community** [NSC20]. **Compact** [CGY⁺14]. **comparators** [YE07]. **Comparing** [Man15, SCF04]. **Competition** [Ano10a]. **Compilation** [RAD⁺23]. **Compiler** [AFG⁺24, DV13, UKM02, WLDN19]. **Compiler-Assisted** [DV13]. **Compiler-Enabled** [UKM02]. **Complementary** [SYC07]. **Complex** [ACG⁺07, ZL18a]. **Complexity** [GG17, LX08]. **Comprehensive** [NS15]. **Compressed** [CEA18]. **Compressing** [PV06]. **Compression** [FPA⁺21, JJP⁺22, MM03, MVJ17, PBO⁺15]. **CompressPoints** [CEA18]. **Computation** [ACSV02, MLA⁺14, YHM17, ZB19]. **Computational** [SAA⁺23]. **Computations** [BY17]. **Compute** [GIH⁺24, JLRA18, LYL⁺16, PL10]. **Compute-in-SRAM** [GIH⁺24]. **Compute-Intensive** [LYL⁺16]. **Computer** [AKK16, Ano08c, Ano09a, Ano09l, Ano09m, Ano10f, Ano10l, Ano10a, Ano10n, Ano10m, Ano11i, Ano12j, Ano13j, Ano14a, Ano14b, Ano14e, Ano14f, Ano15b, Ano15d, Ano15c, Ano15e, Ano15f, Ano15g, Ano15a, Ano16a, Ano16b, Ano17, Ano18, Ano19, Ano20, Ano21, Ano22, BVL09, Eec22, Gau09, KL02, Ska13, TXD⁺23, Ano10c]. **Computers** [AG17, DL20, MTH11, Ano10b]. **Computing** [BSD⁺19, BREM08, DL19, GJ21, JKK⁺21, JAM17, KNG⁺18, KDL23, LHPR23, LJM⁺14, Man15, WLN22, Wu14, ZL17]. **Concurrency** [ZWL15]. **Concurrent** [ODKK18, SK21, ORS⁺06]. **Condition** [XYZ15]. **Conditions** [KCPG18]. **Conference** [Ano15h, Ano10g, Ano12c]. **Confidence** [PL10]. **Confidentiality** [HH22]. **Configurable** [YLK21]. **Configuration** [NR21]. **Configuring** [MSA19]. **conflict** [Zha06]. **Congestion** [GF16]. **Congestion-Insensitive** [GF16]. **Connected** [Ano10f, Ano13j]. **Conquer** [CLCG14]. **conscious** [CMLV03]. **Considering** [MA19]. **Consistency** [SJM02, ZLS10]. **Constrained** [GO15, KPEC10]. **Consumption** [BKA⁺09, FHL⁺10]. **Content** [KWL⁺17, Yav24]. **Content-Based** [KWL⁺17]. **Contention** [ASSK21, SBVB17, TV02, WJFH11]. **Contents** [Ano14g, Ano14h, Ano15j, Ano15k, Ano16n, Ano16o, Ano12h, Ano16p]. **Context** [SRH20]. **Continuous** [SRT12]. **Control** [KKK13, KKL⁺23, LGLK17, NHKR19]. **Control-Flow** [KKL⁺23]. **Controlled**

[ALSJ09, RCS15]. **Controller** [LLPC19, MGHP20, PDGV16]. **conversion** [RB14]. **Convolutional** [GG17, LHZ19, SW19, YKP⁺22]. **Cool** [UKM02]. **Cool-Fetch** [UKM02]. **Cooperative** [CV15, YJZ15]. **Coordinated** [NHKR19]. **Copies** [EE16]. **Coprocessor** [DEC⁺18, Jun17]. **Copying** [KLWJ21]. **Core** [BHL⁺18, BEA⁺13, CVP12, CXS18, DD18, EOA⁺23, FJ08, GBK⁺09, IXS18, Jun17, KFJ⁺03, LMT⁺09, LA16, MNU⁺15, NPS21, NSF⁺18, PKKK23, PHBC18, PL15, SW16, SSS⁺21, SMY15, XYMY16, ZLAE17, SPAP10]. **CoreNap** [PKKK23]. **Cores** [NS15]. **Corollaries** [CM08]. **Correct** [JSDK13, KRB⁺13]. **Correction** [EE16]. **Correlating** [GBS⁺20]. **Correlation** [SfCL03, SW19]. **Cost** [DKD07, MAT17, NS15, ZNTJE23]. **Count** [VGMSLN⁺18]. **Counter** [FBN⁺24, KMJ18, LLSA18, SJM17, RZ06]. **Counter-Based** [FBN⁺24, SJM17]. **Countermeasure** [BGS⁺20]. **Counters** [WLWZ19]. **counting** [Rot08]. **Cover** [Ano08c, Ano11c, Ano11d, Ano11f, Ano11e, Ano16e, Ano16f, Ano16g, Ano16h, Ano16i, Ano16j, Ano08b, Ano09j, Ano09k, Ano10j, Ano10k, Ano11g, Ano11h, Ano12d, Ano12e, Ano12h, Ano12i, Ano12j, Ano13c, Ano13d, Ano13f, Ano13g, Ano16c, Ano16p]. **Cover2** [Ano08a, Ano09h, Ano09i, Ano10h, Ano10i, Ano12f]. **Cover3** [Ano12g]. **Cover4** [Ano09l, Ano09m, Ano10l, Ano10m]. **Covert** [KWKK18, NAG17]. **CPI** [EHDH18]. **CPS** [Ano10g, Ano12c]. **CPU** [CFM⁺03, FLSZ17, HDAS18, LMC⁺09, NMS14, PHO⁺15]. **CPUs** [KCPG18]. **Creating** [MKMJ23]. **Critical** [BGZT22, GKK⁺22, ODKK18, PKKK23, TOIS17, ZAK⁺17]. **Criticality** [KP21]. **Critique** [MLA⁺14]. **Cross** [LEBM20, SHK15]. **Cross-Layer** [SHK15]. **Cross-Stack** [LEBM20]. **Crossbar** [KZY⁺19, ZL17]. **Cryogenic** [RCK21, UTT⁺24]. **Cryptojacking** [LEBM20]. **CSDP** [Ano10d]. **Cube** [JC17, JPC18]. **Customization** [LZD⁺23]. **CXL** [SAA⁺23]. **CXL-Memory** [SAA⁺23]. **Cyber** [Ano16d, KWB⁺20]. **Cyber-Physical** [KWB⁺20]. **Cybersecurity** [Ano15h]. **Cycle** [JC17, KHB⁺19, LYR⁺20, MJBD11, MMAAK21, RL17, RCBJ11]. **Cycle-Accurate** [JC17, KHB⁺19, LYR⁺20]. **Cycle-Level** [MMAAK21]. **Cyclic** [CTNL16].

D [RMMLK16, ZBA⁺20]. **DAEGEN** [WLDN19]. **Dagger** [LAX⁺20]. **DAM** [SSVS21]. **DAMARU** [KYP21]. **Danger** [SKTC05]. **Dark** [CMP⁺14, DXSS15, TNC19]. **Data** [AG17, AD06, ASK⁺21, Ano16k, BLKSA17, BBZ⁺19, DK16, FPA⁺21, GBS⁺20, HCK⁺21, HLH16, HH22, Jac16a, KP21, KPKK20, KWL⁺17, KJK21, KLR24, KLZ12, LPK16, LZL⁺20, MCM13, MAT17, MVJ17, MSE⁺17, NSF⁺18, RL17, RMA⁺20, VMP⁺16, YKP⁺22, ZZW⁺22]. **Data-Aware** [FPA⁺21]. **Data-Dependent** [KWL⁺17]. **Database** [CSSU20]. **Datacenter** [DSVK12, DK13, KQD18, LMT⁺09, LLS⁺15]. **Datacenters** [SG14]. **Dataflow** [AFG⁺24, KLCA21, WLL⁺22]. **Datatype** [WKE12]. **Day** [RTKQ21]. **DC** [MDSG20]. **DCC** [KLS11]. **DDMR** [GWR08]. **Deadblock** [SSVS21]. **Deadlock** [LX08, XL07, XYZ15]. **Deadlock-Free** [XYZ15]. **Debugging** [CVP12]. **Decay** [JDK⁺02]. **Decoder** [YWG17]. **Decomposition** [LCKA23]. **Decomposition-Based** [LCKA23]. **Decongest** [WMZY17]. **Decoupled** [IXS18, KJK21, PTND24, WLDN19]. **Decoupling** [DSVK12, SLC03]. **Deduplicating** [SMLS15]. **Deduplication** [APK⁺18]. **Deep** [GMM⁺19, HLR21, JE22, JKK⁺21, JAM17, KHS⁺24b, KR18, LLPC19, LTL23, NHKR19, RMM24, SCB⁺20].

Deeply [ILXY18a, ILXY18b]. **Defending** [LEBM20]. **Defense** [MPA⁺18, WYY⁺23]. **Delay** [Cit04, SD04]. **Demand** [MHAD15]. **DeMM** [PTND24]. **Demotion** [MDK⁺23]. **Demystifying** [Mic13]. **Denial** [KYP21]. **Denial-of-Service** [KYP21]. **Dense** [WMZY17]. **Dependable** [KLS11]. **Dependence** [GGS19, TOIS17]. **Dependency** [PS17]. **Dependent** [KWL⁺17, MCM13]. **Design** [AS18, Ano10a, ACG⁺07, CTL⁺20, HRF⁺11, HBW⁺23, KNG⁺18, KWB⁺20, LKA15, LLP19, PLK⁺23, SJS24, SKK22, TASA13, TDO16, VMP⁺16, WL16, YHM17]. **designed** [DCG12]. **Designs** [KSO⁺16, XHG⁺19]. **Detailed** [XCW⁺19, YLK21]. **Detect** [WLWZ19]. **Detecting** [LG20, YE07]. **Detection** [KWL⁺17, KJS⁺19, LX08, MMR17, NS15, XL07, ZL18a]. **Detection-Based** [KJS⁺19]. **Determining** [BHY⁺19]. **Determinism** [RSO21]. **Deterministic** [Man15, Mic20, ODKK18]. **Development** [ACG⁺07]. **Device** [HSUS11]. **Devices** [GLH⁺20, WLZZ23]. **Die-Stacked** [SFFG⁺19]. **Differential** [BS17, GMPMC⁺23]. **Digital** [Ano09a, Ano10c, SPHS22]. **Dimensional** [RL08]. **DIMM** [ALSJ09]. **Direct** [CF24, JLS⁺23, NSF⁺18, Zha06]. **Direct-Coding** [CF24]. **direct-mapped** [Zha06]. **Directed** [PGJ12, ZMC17]. **Directional** [LCHL20]. **Directory** [HR10]. **Disaggregated** [Vol21]. **Discovering** [BGZT22, NBW⁺23]. **Discrete** [SRT12]. **Discrete-Continuous** [SRT12]. **Disintermediated** [BDJ06]. **Disk** [YNS⁺08]. **Distance** [BY17]. **Distinguish** [Ano10d]. **Distributed** [AKK16, CZYY11, FD08, MGH⁺22, SSS⁺21, SLKD14, SB18, SRLP09, YJZ15, YP23]. **Distribution** [SK21]. **Disturbance** [MVJ17, WMZY17, WLWZ19]. **Divergence** [ZTS16]. **Divergent** [WJA⁺19]. **Diversity** [TDO16]. **Divide** [CLCG14, ZKW12]. **Divide-and-Conquer** [CLCG14]. **DMA** [MAHK18]. **DNA** [CF24, HKO⁺22, KHS⁺24a]. **DNN** [HCK⁺21, JKK⁺21, KPPK21, MMAAK21, NR21, SBQK21, YP23]. **DNNs** [KKJ⁺22, RAD⁺23]. **Domain** [GGM⁺16, ST20]. **Domain-Specialized** [ST20]. **Dot** [AS18]. **Down** [EGWM14]. **DRACO** [SMLS15]. **DRAM** [EHH21, ILXY18b, JY24, KWL⁺17, KNQ15, KYM16, KKKH18, KKLL22, LLKS12, LKK19, LYR⁺20, LTB⁺24, MCY⁺12, MAT17, MGHP20, NBW⁺23, OKS⁺15, PPA⁺24, SSSM18, SKS⁺15, SHB⁺15, SJM17, SPHS22, SCR⁺17, TMNK19, WLWZ19, WSVS22, XGH⁺22, Yav24, YYK⁺18, ZTRA22]. **DRAM-CAM** [WSVS22]. **DRAM-NVM** [KKLL22]. **DRAMA** [FFAMK15, Yav24]. **Dramaton** [PPA⁺24]. **DRAMs** [ALSJ09]. **DRAMSim2** [RCBJ11]. **DRAMsim3** [LYR⁺20]. **Drive** [SYC14]. **Driven** [MLM⁺06]. **Drives** [JZA⁺18, KKL20]. **Dual** [GWR08, MTT12]. **Due** [RCS15]. **Duplication** [KRB⁺13, MVJ17]. **DVFaaS** [TMSX23]. **DVFS** [CLCG14, NHKR19, RCS15, TMSX23]. **Dynamic** [CFM⁺03, GWR08, GMM⁺19, HCM10, JMKP07, JMKP08, KK21, KCP⁺19, KDS22, LLJK23, LMK06, MHAD15, MCRV07, RMMLK16, SPJ02, SCF04, SKD09, YC15, ZB19]. **Dynamically** [MSA19, WTSW21]. **e-Health** [TS24]. **eADR** [HH22]. **eADR-Based** [HH22]. **Early** [NBH13]. **Early-Stage** [NBH13]. **EARtH** [EGWM14]. **Easy** [MKD⁺23, Ano12k]. **ECC** [RK22]. **Ecosystem** [AWD⁺18]. **Edge** [DL19, KKL⁺23, SJS24, GGS19]. **Edition** [DK13]. **Editor** [Eec13, Gau09, Mar13a, Ska09a, Ska10a, Ska11a, Ska13]. **Editor-in-Chief** [Eec13, Gau09, Mar13a, Ska10a, Ska11a, Ska13]. **Editorial**

[Ano08a, Ano09h, Ano09i, Ano10h, Ano10i, Ano14a, Ano14c, Ano15b, Ano15c, Mar13b, Ska10a, Ska11a]. **Editors** [Mar13a, Eec13]. **eDKM** [CVF⁺24]. **Effective** [AGK21, HRF⁺11]. **Effects** [MTT12]. **Efficiency** [HA24, IXS19, JSLW20, KCP⁺19, KQD18, LLS⁺15, SKTC05, VHN15, MWK⁺06]. **Efficient** [AYL22, AG17, ALSJ09, BLKSA17, BDBS⁺08, BGP⁺17, CGY⁺14, CVF⁺24, CLCG14, CHK⁺18, CXS18, DM06, GDF⁺04, HMCP16, HR10, JSDK13, JJP⁺22, KP21, KHS⁺24a, KDL23, LAX⁺20, LWM20, MCY⁺12, MJBD11, OKS⁺15, PKKK23, SRV⁺19, SKS⁺15, TLG⁺11, TWI⁺24, TS24, WCK08, YHM17, YP23, ZL18b, ZSLR14, SPJ02]. **Efficiently** [LJ04]. **EH** [SGBE18]. **Electromagnetic** [HDAS18]. **Emanations** [HDAS18]. **Embedded** [BDBS⁺08, CLJ⁺02, DS09, GGM⁺16, GRCV02, ILG10, MLC24, MAHK18, PPG⁺17, RADZ19, SKA⁺20, TLG⁺11, YC15]. **Embedding** [KKJ⁺22, LQYF23]. **Embedding-Aware** [LQYF23]. **Embedding-Based** [KKJ⁺22]. **Emerging** [SQ23, WJA⁺19]. **Employing** [LGLK17]. **Enabled** [KKL20, UKM02, ZL17]. **Enabling** [MCY⁺12, MMAAK21, SRS20, SMZ18, WLN22]. **Enclave** [NK22]. **Encrypted** [LGLK17]. **Encryption** [KMJ18, RM18]. **End** [GF16, HXL⁺22]. **End-Point** [GF16]. **End-to-End** [HXL⁺22]. **Endurance** [PLK⁺23, YFPF14]. **Energy** [ALSJ09, BKA⁺09, BDBS⁺08, CV15, CM08, CLCG14, CXS18, DL20, EGWM14, GJ21, GO15, HA24, JSLW20, JSDK13, KP21, KQGS16, KDL23, KKL⁺15, KPEC10, LJM⁺14, PKKK23, SGBE18, TLG⁺11, VHN15, Wu14, ZVYW03, ZL18b, ZSLR14]. **Energy-Constrained** [KPEC10]. **Energy-Efficiency** [HA24, VHN15]. **Energy-Efficient** [BDBS⁺08, KP21, KDL23, TLG⁺11, ZSLR14]. **Energy-Harvesting** [DL20, GJ21, SGBE18]. **Enforced** [MS16]. **Engine** [LTL23, OK22, PTND24]. **Engines** [NK22]. **Enhance** [FJ08, SJM02, TMSA16]. **Enhanced** [KRB⁺13, TOIS17, WCK08]. **enhancement** [Zho06]. **Enhancing** [AQ24, GLJ⁺21, HBW⁺23, VMP⁺16]. **Ensuring** [HH22]. **Entangling** [RJ20]. **Enterprise** [LHCK22]. **Entropy** [Cit04]. **Environment** [ACG⁺07, CVP12, TXD⁺23]. **Environments** [KKH14]. **Epoch** [CNHH15]. **Equal** [Eec24]. **Equal-Time** [Eec24]. **Equal-Work** [Eec24]. **Equality** [YHY⁺22]. **Equations** [BS17, GMPMC⁺23]. **Era** [CMP⁺14, SSS⁺21]. **Error** [EE16, EUVG06, MMR17, NBW⁺23, NS15, PL15, RTKQ21, Vol21, WLWZ19]. **Errors** [GSG⁺17, KRB⁺13, YE07]. **Estimate** [SW16]. **Estimating** [CFM⁺03]. **Estimation** [FAR⁺23]. **Evaluate** [EE14, KKL⁺15]. **Evaluating** [KKL⁺07, LJ04, WLL17]. **Evaluation** [CEA18, KSO⁺16, SJA⁺17]. **Evasive** [LG20]. **Exact** [WSVS22]. **Example** [GRCV02]. **Exascale** [Jac16b, Jac16a]. **Exceeding** [SfCL03]. **Exchange** [NSF⁺18]. **Executed** [MKSP05, WB14]. **Execution** [AWD⁺18, BBZ⁺19, CSSU20, HMCP16, IXS19, KKL⁺15, LLD⁺18, MLK15, MKSP05, NFAE19, ODKK18, TXD⁺23, ZTS16]. **Existing** [EE16]. **Expander** [HCK⁺21]. **Expectations** [YMBA19]. **Expected** [VGMSLN⁺18]. **Experience** [Ano16k, CZYY11]. **Expert** [PB16]. **Explaining** [MCRV07]. **Explicit** [BHD09]. **Exploit** [ZLAE17]. **Exploiting** [ÇE14, Cit04, EE16, EUVG06, GRCV02, GG11, KWKK18, KYW⁺24, LKK19, Mic20, yPSS⁺10, SBQK21, XJ09, ZSLR14]. **Exploration** [LLPC19, SGBE18]. **Explore** [BSD⁺19]. **Exploring** [BHL⁺18, CSSU20, HSUS11, NPBS23, SHJW21, WLDN19]. **Extending** [JP13, MV15, VMS17]. **Extensible** [KYM16, LTB⁺24, MGHP20]. **Extensions** [KYW⁺24]. **Extra** [SMLS15].

EZ [ZL18b]. **EZ-Pass** [ZL18b].

FaaS [TMSX23]. **Fabric** [ZL17]. **Facilitate** [ZLS10]. **Failures** [KWL⁺17, SG14]. **Fairness** [MA19, VS11]. **Fast** [KYM16, LGLK17, MKD⁺23, SMZ18, SHB⁺15, SKS⁺24, YP23]. **FastDrain** [ZKH⁺20]. **Fat** [Ant09, GVG⁺08]. **Fat-tree** [Ant09, GVG⁺08]. **Fault** [GDF⁺04, HRF⁺11, ZKF⁺18, Zho06]. **Fault-Aware** [ZKF⁺18]. **Fault-Tolerant** [GDF⁺04, HRF⁺11]. **Faults** [OKS⁺15, SKS⁺15]. **Feature** [YSL⁺21]. **FESSD** [LGLK17]. **Fetch** [MSA19, UKM02, AGJ18, PGJ12, UKM02]. **Fighting** [AMW15]. **File** [EE16, JEAG⁺19]. **Filter** [GF16, HKO⁺22]. **Filtering** [CXS18, KHS⁺24a]. **find** [Ano12k]. **Fine** [BRUS21, MKM17, MCY⁺12, MKP⁺24, WYM⁺16]. **Fine-Grained** [BRUS21, MKP⁺24, WYM⁺16]. **Fine-Granularity** [MCY⁺12]. **Firmware** [BGL⁺23]. **First** [CAPS09, Eec22]. **First-Order** [Eec22]. **Fit** [LWB13]. **Fixed** [GRCV02]. **Flash** [IKW⁺20, KJK21, LKA15, LZLX15, yPSS⁺10, SYC14, YNS⁺08]. **Flash-Based** [LZLX15, yPSS⁺10, SYC14]. **Flash/FRAM** [YNS⁺08]. **Flattened** [KBD07]. **Flexibility** [KPPK21, TND⁺21]. **Flexible** [LQYF23, LWB13, XCW⁺19]. **Flexion** [KPPK21]. **FlexScore** [TND⁺21]. **Floating** [ACSV02, DKD07, LTL23]. **Floating-Point** [DKD07, LTL23]. **Flow** [Hos18, KKK13, KKL⁺23, MSE⁺17]. **Flow-Based** [Hos18]. **Footprint** [SW16]. **Foreword** [GPS06]. **Format** [LZD⁺23]. **Forward** [ASSK21, KKL⁺23, NB24]. **Forward-Edge** [KKL⁺23]. **Forwarding** [BHD09]. **FPGA** [FLSZ17, KLR24, LAC14, LZL⁺20, MGH⁺22, PP12]. **FPGA-Accelerated** [KLR24]. **FPGA-Based** [MGH⁺22, LAC14]. **FPGAs** [LCHL20, RAD⁺23, SKK22]. **Fractal** [ZLS10]. **FRAM** [YNS⁺08]. **Framework** [AFG⁺24, BSD⁺19, BVL09, CYAW20, JJP⁺22, KLZ12, LHZ19, LWB13, MHM⁺24, SKK22, TMNK19, LHWB10]. **Free** [GFAHSA24, PS17, XYZ15]. **Frequency** [CTNL16, MLM⁺06, Mic20, YC15]. **Friendly** [LHPR23, LCKA23, PZX15]. **Front** [Ano08b, Ano09j, Ano09k, Ano10j, Ano10k, Ano11g, Ano11h, Ano12h, Ano12i, Ano13f, Ano13g]. **FTL** [SMLS15]. **Fully** [ZL17]. **Function** [LLKS12]. **Functional** [CAPS09, DCG12]. **Functional-First** [CAPS09]. **Functions** [TD02]. **Fusion** [LYY⁺21]. **Fuzzy** [ACSV02].

G [NS15]. **Gap** [ILXY18b]. **GATE** [YQL⁺24]. **Gather** [SKS⁺24]. **Gating** [CTNL16, LMT⁺09, ZL18b]. **GCMS** [WJFH11]. **GCN** [YSL⁺21]. **GCNs** [LYY⁺21, YCD⁺20]. **gem5** [RSRT19, AKK16, PHO⁺15, VRFT24]. **gem5-accel** [VRFT24]. **gem5-gpu** [PHO⁺15]. **GEMM** [LWM20]. **General** [DPP23, LZD⁺23, WSVS22]. **General-Purpose** [WSVS22]. **Generalizability** [GDU⁺24]. **Generalized** [AS18, CTL⁺20, GO15, MMY⁺14]. **Generate** [MHM⁺24]. **Generation** [BVL09, GMMC15, JLKK23, SKK22]. **Generative** [CPK⁺23]. **Generators** [SJS24]. **Genome** [LJ18]. **Geomean** [Eec24]. **Global** [KK21, MPSS17, WJFH11]. **Globally** [SDTG04]. **GNN** [QYZ⁺24]. **GNNs** [WYY⁺23]. **Goal** [TDO16]. **GP** [JJP⁺22]. **GP-GPU** [JJP⁺22]. **GPGPU** [CCWY17, LLKS12, NS15, SW16, ZCG18]. **GPGPUs** [NAG17, SSSM18, ZLAE17, ZWL15]. **GPU** [ABC⁺19, IXS19, JSLW20, JEAG⁺19, JJP⁺22, KLKK14, KCP⁺19, LSJ⁺19, RASW19, WCYC09, WJA⁺19, XWG⁺14, YCD⁺20, PHO⁺15]. **GPU-NEST** [JSLW20]. **GPUs** [HA24, HCK⁺21, HCK22, HXL⁺22, NMS14, NSF⁺18, PGR⁺23, PBO⁺15, WYM⁺16, WYY⁺23, ZYZ⁺22,

YC15, ZTS16, ZNTJE23, ZZW⁺23]. **Grain** [MKM17, ZM07]. **Grained** [BRUS21, LYL⁺16, MKP⁺24, WYM⁺16]. **GraNDe** [YKP⁺22]. **Granular** [MNFI20, YJZ15]. **Granularity** [MCY⁺12]. **Graph** [AYL22, BY17, BHL⁺18, FSO⁺22, GKK⁺22, LKR21, NSC20, NGS15, ST20, SKS⁺24, SHJW21, TOIS17, YQL⁺24, YKP⁺22, ZLM⁺20, ZZW⁺22]. **Graph-Based** [NGS15]. **Graph-Processing** [ST20]. **Graphs** [GGS19]. **GraphSCC** [NSC20]. **Greedy** [DC18]. **GreenRouter** [KWL13]. **Guarantee** [NB24]. **Guard** [MKMJ23]. **Guessing** [WTSW21]. **Guiding** [BY17].

HAD-TWL [KJS⁺19]. **Half** [MTT12]. **Half-Speed** [MTT12]. **Halt** [EGWM14]. **Halting** [ZVYW03]. **Hammer** [LKP⁺23, LHPR23]. **Hammering** [KNQ15, LLSA18, SJM17]. **Hardware** [AGJ18, AW15, CTJ⁺17, CWK⁺22, CV15, CKA20, DVAE18, DD18, GKK⁺22, JLKK23, KP21, KKL⁺23, KH18, LHPR23, LAS22, LMK06, LCW⁺16, LYY⁺21, LCKA23, LAM⁺22, MLK15, MKM17, MS16, NB24, NGS15, OK22, PB16, SK21, SPHS22, WJFH11, WLL17, XL07, YCH24, ZS18]. **Hardware-Assisted** [CKA20, KKL⁺23]. **Hardware-Friendly** [LHPR23, LCKA23]. **Hardware-Software** [CV15]. **Hardware/Software** [MKM17]. **Harmonic** [Eec24, PL10]. **Harnessing** [GBS⁺20]. **Harvesting** [DL20, GJ21, SGBE18, Wu14]. **Hashing** [SMZ18]. **HBM3** [GLJ⁺21]. **HCI** [VMP⁺16]. **Headers** [JLKK23]. **Health** [TS24]. **Heavy** [SSTS17]. **Heterogeneity** [APK⁺21, MTH11]. **Heterogeneity-Aware** [APK⁺21]. **Heterogeneous** [AEJE17, BRUS21, DL20, FLSZ17, GO15, GMM⁺19, HCK22, KFJ⁺03, LLS⁺15, MMY⁺14, PHO⁺15, TDO16, TMNK19, ZBA⁺20, ZKW12]. **Heterogeneous-ISA** [BRUS21]. **Heterogeneous-Reliability** [TMNK19]. **HeteroSim** [FLSZ17]. **Heuristics** [MGI14]. **HGNNs** [YZY⁺22]. **Hiding** [CST⁺04]. **Hierarchical** [BSBD⁺08, SKA⁺20]. **Hierarchy** [BHL⁺18, YMG14, ZM07]. **High** [CTL⁺20, DPC16, JSDK13, KKK13, KL18, LTL23, PLK⁺23, PP12, RMMLK16, RB14, SKK22, SD04, SYC14, SRLP09, SHJW21, TASA13, TS24, YFPF14, YNS⁺08, ZVYW03, LHWB10]. **High-Bandwidth** [KL18]. **High-Endurance** [PLK⁺23]. **High-Level** [PP12]. **High-Performance** [CTL⁺20, DPC16, LTL23, PLK⁺23, RMMLK16, SKK22, SHJW21, TASA13, ZVYW03, SYC14, LHWB10]. **High-Throughput** [KKK13, SRLP09]. **Highly** [KL18, RMA⁺20]. **Highly-Banked** [RMA⁺20]. **HiLITE** [SKA⁺20]. **Hit** [VGMSLN⁺18]. **HLS** [KDS22]. **HMC** [JPC18]. **HMC-MAC** [JPC18]. **Holes** [AEJE17]. **Holistic** [JZA⁺18, KSO⁺16]. **Homogeneous** [MTH11]. **Horizontal** [GG11]. **Hot** [KJS⁺19, WMZY17]. **HPC** [KR18]. **Hungarian** [EOA⁺23]. **HW** [APK⁺18, DCG12]. **HW-Based** [APK⁺18]. **HW/SW** [DCG12]. **Hy** [NPS21]. **Hy-Sched** [NPS21]. **Hybrid** [JC17, JPC18, JP13, KKLL22, KSB19, LMK06, MCY⁺12, MV15, SSVS21, SRT12, YNS⁺08, YYK⁺18]. **Hyperthreading** [NPS21]. **Hyperthreading-Aware** [NPS21]. **Hyervisor** [PPG⁺17]. **hysteresis** [RZ06].

I/O [JLS⁺23, KLWJ21, LKA15, LKKS15, MAHK18, SYC14]. **I/O-Intensive** [JLS⁺23]. **IBM** [LCW⁺16]. **Ideal** [ALKSA19]. **Ideas** [JLA16]. **IDIO** [ASK⁺21]. **IEEE** [Ano08c, Ano09a, Ano09l, Ano09m, Ano10f, Ano10l, Ano10a, Ano10n, Ano10m, Ano11i, Ano12j, Ano13h, Ano13i, Ano13j, Ano14e, Ano14f, Ano15f, Ano15g, Ano16l, Ano16m, Ano10b, Ano13e, Ano14a, Ano14b, Ano14c, Ano14d, Ano15b, Ano15d, Ano15c, Ano15e, Ano15a, Ano16d, Ano16a,

Ano16b, Ano17, Ano18, Ano19, Ano20, Ano21, Ano22, Gau09, Ska13]. **IF** [RB14]. **IF-conversion** [RB14]. **IK** [YCH24]. **IMEC** [ZL17]. **Imitation** [SKA⁺20]. **Immediate** [EHH21]. **Immediate-Response** [EHH21]. **Impact** [FHL⁺10, GSG⁺17]. **Impacts** [WKE12]. **Implementation** [LAM⁺22, WLL⁺22]. **Implementing** [JDK⁺02, TMNK19]. **Implication** [LKR21]. **Implications** [DK16, GD18, OSH16, QYZ⁺24, ZLM⁺20]. **Importance** [GDU⁺24]. **Improve** [KH18, KQD18, MMR17, WMJM23, XJ09]. **Improved** [DKD07, PGR⁺23]. **Improvement** [MA19]. **Improving** [CCWY17, CZYY11, HA24, IXS19, ILXY18a, KCP⁺19, LLS⁺15, MSA19]. **In-DRAM** [MAT17, XGH⁺22]. **in-Hardware** [SK21]. **In-Line** [LAC14]. **In-Memory** [CSSU20, CHK⁺18, LAS22, SRV⁺19, SKS⁺24, WLN22, ZL17]. **In-network** [EPS06]. **In-Order** [EHdSH20, HEDH21, PGJ12]. **In-SRAM** [SRS20]. **Inbound** [ASK⁺21]. **Including** [DRGA12]. **Increasing** [ÇE14]. **Incremental** [MAT17]. **Independent** [DS09, LKKS15, WLZZ23]. **Independently** [ALSJ09]. **Index** [Ano11a, Ano12a, Ano13a, Ano15a, Ano16a, Ano16b, Ano17, Ano18, Ano19, Ano20, Ano21, Ano22, WMJM23]. **Indirect** [JMKP07, JMKP08]. **Induced** [DXSS15]. **Industry** [ILNS20]. **Inference** [CPK⁺23, DL19, JSLW20, KDL23, KKL20, KYW⁺24, LWM20, MMAAK21, NR21]. **Inference-Enabled** [KKL20]. **Infinity** [WLN22]. **Information** [Ano08d, Ano09n, Ano09o, Ano10o, Ano10p, Ano14b, Ano14d, Ano15d, Ano15e, MLC24, Ano11i, Ano11j]. **Infrastructure** [AKK16]. **Initial** [ACSV02]. **Inline** [APK⁺18]. **Innovating** [KWL13]. **Inputs** [BEA⁺13]. **Insensitive** [GF16]. **Insertion** [JTG23]. **Inspired** [OKS⁺15, SKS⁺15]. **Instead** [Eec24]. **Instruction** [ALKSA19, BSBD⁺08, GIH⁺24, ILNS20, KP21, MMR17, MSA19, RYSN04, RJ20, WCZ⁺12, Zha06]. **Instructions** [ASSK21, MKSP05, WB14]. **Integrated** [NMS14, OK22]. **Integrating** [FAR⁺23]. **Integration** [Jun17, ZBA⁺20]. **Integrity** [KKL⁺23, RADZ19, SB18]. **Intel** [CLCG14, KYW⁺24, MDSG20]. **Intelligence** [Ano14c, Ano14d]. **Intelligent** [BGL⁺23]. **Intensive** [JLS⁺23, LYL⁺16, SAA⁺23]. **Inter** [GGM⁺16, LA16, NSF⁺18, RASW19, RMA⁺20, SPAP10, UTT⁺24, ZTS16, ZLAE17]. **Inter-Bank** [RMA⁺20]. **Inter-Core** [LA16, NSF⁺18, ZLAE17]. **Inter-Domain** [GGM⁺16]. **Inter-GPU** [RASW19]. **Inter-Socket** [SPAP10]. **Inter-Temperature** [UTT⁺24]. **Inter-Warp** [ZTS16]. **Interaction** [HSUS11]. **Interconnect** [CGY⁺14, KG10, SRV⁺19]. **Interconnection** [Ant09, GVG⁺08, SPJ02, SD04, GD06]. **Interface** [BHY⁺19]. **Interference** [ASSK21]. **Interleaving** [LLJK23, VD02]. **Intermediate** [LZD⁺23, WXZ⁺21]. **Internal** [NBW⁺23, yPSS⁺10]. **Interpreter** [MSI18]. **Interval** [SKTC05]. **Interval-Based** [SKTC05]. **Intervals** [GWR08, PL10]. **Intra** [SPAP10]. **Intra-Socket** [SPAP10]. **Intrinsic** [MMR17]. **Introducing** [Ano16l, Ano16m, Gau09, Ska13]. **Introduction** [Eec13, Mar13a]. **Intrusion** [ZL18a]. **Intrusive** [PDGV16]. **Invariant** [ASSK21]. **Inverse** [YCH24]. **IP** [KL18]. **IPC** [EE14]. **Irregular** [CLCG14]. **ISA** [BRUS21, KFJ⁺03, MNU⁺15, WXZ⁺21]. **Isolating** [BBZ⁺19]. **Isolation** [ODKK18]. **Issue** [MVJ17, RYSN04]. **Issuing** [NBW⁺23]. **Jacobian** [YCH24]. **JANM** [YCH24]. **JANM-IK** [YCH24]. **Jaseci** [MKD⁺23]. **Java** [DS09]. **JavaScript** [VP16]. **Jobs**

[Ano10n]. **Journaling** [BGL⁺23]. **Jumps** [JMKP07, JMKP08].

Kernel [NMS14]. **Key** [KKLL22, PLK⁺23]. **Key-Value** [PLK⁺23]. **Kinematics** [YCH24]. **kmer** [JY24]. **Kobold** [BSMB23]. **KSM** [ZCG18]. **KV** [PJ22]. **kW** [Jac16a].

L1 [BLKSA17, PHBC18, VMP⁺16]. **L2** [CST⁺04]. **L3** [FJ08]. **LA-LLC** [ZLAE17]. **LADIO** [JLS⁺23]. **Language** [CVF⁺24, KYW⁺24, LZD⁺23]. **Large** [CVF⁺24, CPK⁺23, DRGA12, DSVK12, HCM10, JLA16, KYW⁺24, LKR21, PLK⁺23, PPA⁺24, SG14]. **Large-Key** [PLK⁺23]. **Large-Scale** [DRGA12, DSVK12, LKR21]. **Last** [JTG23, KYP21, LKP⁺23, YFPF14, ZLAE17]. **Last-Level** [JTG23, KYP21, LKP⁺23, ZLAE17]. **Latency** [KJS⁺19, KLWJ21, LTL23, NPBS23, PKKK23, SCR⁺17, ZAK⁺17, ZZW⁺23]. **Latency-Critical** [PKKK23, ZAK⁺17]. **Latency-Versatile** [LTL23]. **Law** [CM08, VMS17]. **Layer** [KSO⁺16, SHK15]. **Layout** [ALKSA19, KHS⁺24a]. **LazyPIM** [BGP⁺17]. **Leakage** [FAR⁺23, JLS⁺23]. **Leakage-Aware** [JLS⁺23]. **Learned** [LKL⁺21]. **Learning** [GDU⁺24, GMM⁺19, HLR21, JE22, KHS⁺24b, LLPC19, RMM24, SKA⁺20, SCB⁺20, WMJM23, YG18, ZZW⁺22]. **Learning-Based** [ZZW⁺22]. **LEO** [RM18]. **Letter** [Ska09a, Ska10a, Ska11a]. **Letters** [Ano14a, Ano15b, Ano15c, Ano14b, Ano15d, Ano15e, Ano15a, Ano16a, Ano16b, Ano17, Ano18, Ano19, Ano20, Ano21, Ano22, Gau09, Ska13]. **Level** [ILXY18a, JTG23, KHS⁺24b, KYP21, LKK19, LKP⁺23, LMJ12, MGI14, MMAAK21, PJ22, PP12, TV02, TMSA16, VE18, YFPF14, ZLAE17, ZCG18, LLLM06, XJ09]. **Leveling** [KJS⁺19, LZLX15, ZKF⁺18]. **Leveraging** [DD18, KG10, KQD18, LMJ12, LLS⁺15,

MXS19, NR21, TMSX23, WZLQ15, ZS18]. **LFSR** [SJS24]. **LFSR-Based** [SJS24]. **Library** [ACG⁺07, Ano09a, Ano10c]. **Life** [RTKQ21]. **Lifetime** [BSD⁺19, HSUS11, JP13, MV15, SMY15]. **Light** [IXS19]. **Light-Weight** [IXS19]. **Lightweight** [CYAW20, LCW⁺24, LAM⁺22, SKA⁺20, ZZW⁺22]. **like** [WCZ⁺12]. **Limit** [KWB⁺20]. **Limited** [AEJE17]. **Limits** [CTJ⁺17, SfCL03]. **Line** [LAC14]. **Linearization** [LHPR23]. **Link** [HRF⁺11, SCF04]. **Links** [SPJ02]. **List** [Ano11b, Ano12b, Ano13b]. **LLC** [KKH14, ZLAE17]. **LLVM** [RSRT19]. **LLVM-Based** [RSRT19]. **LMT** [SJ22]. **Load** [Ant09, GVG⁺08, HR10, ILXY18a, SDTG04]. **Load-Balanced** [Ant09, SDTG04]. **Load-Load** [HR10]. **Locality** [BY17, CCWY17, EF07, GG11, JEAG⁺19, LA16, SfCL03, SRLM20, XJ09, ZLAE17]. **Locality-Aware** [JEAG⁺19, ZLAE17]. **Lock** [MNU⁺15]. **loft** [IPS14]. **LogCA** [AW15]. **Logic** [FD08, TNC19]. **Logic-Based** [FD08]. **Long** [KHS⁺24a, ZZW⁺23]. **Longer** [AQ24]. **LOOG** [IXS19]. **Lookaside** [LMJ12]. **Lookup** [KL18]. **Lookups** [CSSU20]. **Loop** [GRCV02]. **Loops** [GAH⁺23]. **Low** [CLJ⁺02, Cit04, DKD07, GG17, GFAHSA24, KJS⁺19, KLWJ21, MAT17, NS15, PHBC18, RM18, SRS20, YFPF14, ZVYW03, LHWB10, MTT12]. **Low-Cost** [DKD07, MAT17, NS15]. **Low-Energy** [ZVYW03]. **Low-Latency** [KLWJ21]. **Low-Overhead** [SRS20]. **Low-Power** [GFAHSA24, PHBC18, LHWB10]. **LSM** [PJ22]. **LSTM** [MXS19]. **LT** [ZTRA22]. **LT-PIM** [ZTRA22]. **LUT** [ZTRA22]. **LUT-Based** [ZTRA22]. **LV** [LTL23]. **LWE** [LAM⁺22].

MAC [JPC18]. **Machine** [Ano14c, Ano14d, DL19, GDU⁺24, LCW⁺24, YG18].

Machines [GBK⁺09, KWB⁺20, UTT⁺24]. **Main** [Sez10, YYK⁺18]. **Majority** [JY24]. **MajorK** [JY24]. **Making** [YSL⁺21]. **Manage** [MCM13]. **Managed** [GMMC15]. **Management** [CFM⁺03, EGWM14, GMM⁺19, KPKK20, KWKK18, LKK19, LKP⁺23, LMT⁺09, MPPS17, MCY⁺12, MAHK18, MKP⁺24, PGR⁺23, RADZ19, SKA⁺20, SSS⁺21, SMY15, TMSA16, WJFH11, ZAK⁺17]. **Managing** [DOM⁺07, DOM⁺08, JE22]. **Many** [BHY⁺19, CXS18, DXSS15, GBK⁺09, KDS22, NBH13, PHBC18, SSS⁺21, SMY15, XYMY16, ZLAE17, ZZW⁺23]. **Many-Accelerator** [BHY⁺19, DXSS15, KDS22, NBH13]. **Many-Chip-Module** [ZZW⁺23]. **Many-Core** [CXS18, GBK⁺09, PHBC18, SSS⁺21, SMY15, XYMY16]. **Many-Thread** [GBK⁺09]. **Many-to-Many** [ZLAE17]. **mapped** [Zha06]. **Mapping** [EOA⁺23, HLH16, LHZ19, YKP⁺22]. **MapReduce** [IXS18, LYL⁺16]. **Massive** [Mus09, SMZ18]. **Massively** [ADS⁺19]. **match** [YE07]. **Matching** [JY24, PLL08, WSVS22, ZL18a]. **Matrix** [KYW⁺24, LCKA23, MNFI20, PTND24, YKP⁺22]. **MCsim** [MGHP20]. **Mead** [YCH24]. **Mean** [Eec24, LHPR23, PL10]. **Mean-Redistribution** [LHPR23]. **Measuring** [GSG⁺17]. **Mechanism** [BGP⁺17]. **Mechanisms** [RCS15, TVB⁺13, XYMY16]. **Memcached** [LAC14]. **Memoization** [ZS18]. **Memories** [KHB⁺19, KNQ15, KDS22, KZY⁺19, MCY⁺12, RM18, RMA⁺20, RMM24, SM18, WCC14]. **Memory** [ALSJ09, AA19, AMW15, BKA⁺09, BGP⁺17, CSSU20, CYAW20, CKA20, CEA18, CHK⁺18, CMP⁺14, DXSS15, DD18, EHH21, FFAMK15, GSG⁺17, GLH⁺20, HCK⁺21, HKO⁺22, HCK22, IXS18, JC17, JPC18, JSDK13, JJP⁺22, JDK⁺02, JLA16, Jun17, JLRA18, KQGS16, KWL⁺17, KHS⁺24a, KNG⁺18, KLKK14, KL18, KJS⁺19, KPL⁺21, KKLL22, KKJ⁺22, KMJ18, KR18, LAX⁺20, LGLK17, LKK19, LKR21, LLJK23, LAS22, LMK06, LA16, LZLX15, LLPC19, LJ18, LQYF23, MDSG20, MGHP20, MDK⁺23, NBW⁺23, OK22, PS17, PZX15, RMA⁺20, RMM24, RCBJ11, SRV⁺19, Sez10, SPHS22, SKS⁺24, SB18, SAA⁺23, SFFG⁺19, SCB⁺20, TWI⁺24, VE18, VHN15, Vol21, WJFH11, WYL⁺15, WJA⁺19, WLN22, WTSW21, WLZZ23, XWG⁺14, XCW⁺19, Yav24, YQL⁺24, YLK21, YYK⁺18, ZM07, ZL17, ZLS10, ZZJ18, BLM06, SAA⁺23]. **Memory-Centric** [KR18]. **Memory-Divergent** [WJA⁺19]. **Memory-Error** [Vol21]. **Memory-Induced** [DXSS15]. **Memory-Intensive** [SAA⁺23]. **Memory-Level** [VE18]. **Memory-Unaware** [KLKK14]. **Memristor** [KNE⁺14]. **Memristor-Based** [KNE⁺14]. **Merkle** [JLKK23, TWI⁺24]. **Mesh** [RL08, SCL13, XYZ15]. **Meshes** [GDF⁺04]. **Message** [Eec13, GGM⁺16, Mar13a]. **Metadata** [GBS⁺20, MKP⁺24, RADZ19]. **Method** [LPK16]. **Methodology** [CEA18, DM06, GDF⁺04, Hos18, WL16]. **Methods** [WYY⁺23]. **Metric** [KKL⁺07, KPPK21]. **Metrics** [EE14, Mic13, NBH13, PL10, SKTC05, VS11, YMBA19]. **Microarchitectural** [BGZT22, DKD07, MSI18, MMAAK21]. **Microarchitecture** [CNHH15, FAR⁺23, KCB⁺20, WXZ⁺21]. **Microarchitecture-Based** [CNHH15]. **Microarchitectures** [DOM⁺07, DOM⁺08, DPP23]. **Microservices** [GD18, LAX⁺20, LLM⁺21]. **Migration** [SSVS21, SD02, SLKD14]. **MIMD** [WCZ⁺12]. **MIMD-like** [WCZ⁺12]. **Mind** [AEJE17]. **Minimal** [FHL⁺10, RL08]. **Mining** [DK16, SHJW21]. **MinneSPEC** [KL02]. **Mirage** [SQ23, SQ23]. **Misprediction** [SYC07]. **Miss** [EHdSH20].

Misses [CST⁺04, Zha06]. **Mitigate** [VMP⁺16]. **Mitigating** [DXSS15, KNQ15, MTT12, SBVB17]. **Mitigation** [CKZ⁺20, KWL⁺17, PHBC18, SJM17]. **Mitigations** [FBN⁺24]. **MNCaRT** [AWD⁺18]. **Mobile** [LWM20, TLG⁺11, ZSLR14]. **Modal** [HXL⁺22]. **Mode** [KPKK20]. **Mode-Aware** [KPKK20]. **Model** [AW15, BEA⁺13, DL20, Eec22, EHH21, FSO⁺22, KKL⁺15, KYW⁺24, KWB⁺20, LKL⁺21, LHE⁺21, PP12, PZX15, SGBE18, TOIS17, IPS14]. **Modeling** [ABC⁺19, BS17, EHH21, FAR⁺23, GJ21, GGS19, HEDH21, JZA⁺18, KKP⁺18, NBH13, PPG11, RSRT19, SQ23, VE18, WJA⁺19, SCL06]. **Models** [BREM08, CVF⁺24, CPK⁺23, DRGA12, GO15, HBL⁺10, LCKA23, SW16, SPHS22, SJM02]. **Modern** [CWK⁺22, HA24, LTB⁺24, SFFG⁺19, TOIS17]. **Modular** [GWR08, LTB⁺24, WLDN19]. **Module** [ALSJ09, ZNTJE23, ZZW⁺23]. **Monitoring** [DEC⁺18, GMMC15]. **Monte** [SCL06]. **Morphable** [ZL17]. **Morphing** [YSL⁺21]. **Most** [Ano16k]. **Movement** [KJK21]. **MPSoC** [PP12]. **MPSoCs** [KLZ12]. **MPU** [VRS18, XGH⁺22]. **MPU-Sim** [XGH⁺22]. **MQSim** [LHCK22]. **MQSim-E** [LHCK22]. **MRAM** [ILXY18a, ILXY18b, ZBA⁺20]. **MTB** [AGJ18]. **MTB-Fetch** [AGJ18]. **Mth** [MKM17]. **Multi** [AWD⁺18, CVP12, EOA⁺23, EHDH18, FJ08, HXL⁺22, IXS18, JSLW20, JJP⁺22, Jun17, KSO⁺16, KFJ⁺03, LSJ⁺19, MNU⁺15, MMY⁺14, PLL08, PJ22, PL15, RL17, SMZ18, SKK22, SPAP10, VS11, YLK21, ZNTJE23, Zho06]. **Multi-Accelerator** [MMY⁺14]. **Multi-Architecture** [AWD⁺18]. **Multi-Chip-Module** [ZNTJE23]. **Multi-Core** [CVP12, EOA⁺23, FJ08, IXS18, Jun17, KFJ⁺03, MNU⁺15, PL15, SPAP10]. **Multi-Cycle** [RL17]. **Multi-Die** [SKK22]. **Multi-GPU** [JSLW20, LSJ⁺19]. **Multi-Layer** [KSO⁺16]. **Multi-Level** [PJ22]. **Multi-Modal** [HXL⁺22]. **Multi-Prediction** [JJP⁺22]. **multi-processors** [Zho06]. **Multi-Stack** [YLK21]. **Multi-Stage** [EHDH18]. **Multi-String** [PLL08]. **Multi-Tenant** [LSJ⁺19]. **Multi-Threaded** [VS11]. **Multi-Threading** [SMZ18]. **MultiAmdahl** [MMY⁺14, ZKW12]. **Multicore** [ALSJ09, BEA⁺13, CAPS09, DVAE18, DM06, KCPG18, KLS11, Mic13, Mus09, NK22, ODKK18, SRH20, SHK15]. **Multicores** [AEJE17, SK21, VMS17]. **Multidimensional** [JSDK13]. **Multikernel** [WYM⁺16]. **Multilevel** [CF24, PPG11]. **Multimedia** [ACSV02]. **MultiPIM** [YLK21]. **Multiplication** [LCKA23, PTND24]. **Multipplier** [SJS24]. **Multiply** [GG17, JPC18]. **Multiprocessor** [ILG10, PPG11, SLC03, XL07]. **Multiprocessors** [AGJ18, GKKW07, HCM10, LMJ12, MTT12, SD02, MWK⁺06]. **Multiprogram** [EE14]. **Multistage** [Ant09, GVG⁺08]. **Multitasking** [KCP⁺19, ZCG18]. **Multithreaded** [BVL09, DVAE18]. **Multithreading** [AGJ18, KNE⁺14, SHW19]. **My** [ZKW12]. **Nahalal** [GKKW07]. **NAND** [KJK21]. **NAND-Based** [KJK21]. **Nanopore** [LJ18]. **Narrow** [EUVG06, KRB⁺13]. **Native** [MLK15]. **Near** [ALKSA19, FFAMK15, HCK⁺21, HKO⁺22, JKK⁺21, KPEC10, LAX⁺20, LZL⁺20, LQYF23, PPA⁺24, XGH⁺22, YQL⁺24, YKP⁺22]. **Near-Bank** [XGH⁺22]. **Near-Data** [HCK⁺21, YKP⁺22]. **Near-DRAM** [PPA⁺24]. **Near-Ideal** [ALKSA19]. **Near-Memory** [LAX⁺20, YQL⁺24]. **Near-Storage** [JKK⁺21, LZL⁺20]. **Near-Threshold** [KPEC10]. **NearZero** [Jun17]. **Neda** [NSF⁺18]. **Need** [CVP12]. **Neighbor** [NSF⁺18]. **Nelder** [YCH24].

NEST [JSLW20]. **Nested** [HBL⁺10].
Netflix [DK13]. **Network**
 [ASK⁺21, Ant09, CGY⁺14, GFAHSA24,
 GVG⁺08, JAM17, KPKK20, LKR21,
 LZS⁺08, LHZ19, MHM⁺24, PL15, RMA⁺20,
 SCL13, WCK08, XHG⁺19, YQL⁺24, ZL18a,
 EPS06, TASA13]. **Network-on-Chip**
 [CGY⁺14, GFAHSA24, LZS⁺08, PL15].
Network-on-Memory [RMA⁺20].
Network-on-SSD [TASA13]. **Networks**
 [FPA⁺21, GG17, GKK⁺22, HA24, HXL⁺22,
 KBD07, KKK13, KR18, LTL23, MLC24,
 MXS19, MJB11, NHKR19, RL08, RL09,
 RMMLK16, SPJ02, SW19, SD04, XYZ15,
 YHM17, YKP⁺22, ZLM⁺20, GD06].
Networks-on-Chip [RMMLK16].
Neumann [DC18]. **Neural** [FPA⁺21, GG17,
 GKK⁺22, HXL⁺22, JAM17, KR18, LKR21,
 LHZ19, LTL23, MLC24, MXS19, NHKR19,
 SW19, XHG⁺19, YHM17, ZLM⁺20].
Neuromorphic [BSD⁺19]. **Newest**
 [Ano16k]. **Newsletter** [Ano13e]. **Next**
 [GMMC15]. **NICs** [LAX⁺20, MGH⁺22].
Nile [DEC⁺18]. **NMTSim** [GLH⁺20].
NNBench [XHG⁺19]. **NNBench-X**
 [XHG⁺19]. **NoC** [SRLP09, WL16]. **NoCs**
 [DPC16, FHL⁺10, FD08, MCKW10, ZL18b].
NoHammer [LKP⁺23]. **Noise**
 [CKZ⁺20, HDAS18]. **Noisy** [MKMJ23].
NoM [RMA⁺20]. **Non**
 [LKR21, PZX15, PDGV16, RM18, RSO21,
 SM18, VHN15, WZLQ15]. **Non-** [PZX15].
Non-Determinism [RSO21].
Non-Intrusive [PDGV16]. **Non-Volatile**
 [LKR21, RM18, SM18, VHN15, WZLQ15].
Novel [TS24, XL07]. **NUMA** [SJA⁺17].
Number [PPA⁺24]. **NVM**
 [CYAW20, HH22, KKLL22, MV15, PDGV16].
NVMain [PZX15]. **NVMe** [ZKH⁺20].
NVMM [OK22].

O [JLS⁺23, KLWJ21, LKA15, LKKS15,
 MAHK18, SYC14]. **O-Intensive** [JLS⁺23].
Obfuscation [CYAW20]. **Oblivious**
 [SCL13, TD02]. **Odd** [SCL13]. **ODIN**
 [SRLM20]. **Off** [GKK⁺22, RSO21]. **Offer**
 [Ano10e]. **Offlining** [LKK19]. **offs**
 [BSD⁺19]. **On-Chip**
 [GGM⁺16, KBD07, KKK13, KDS22, KLZ12,
 LGLK17, MJB11, ZM07, WCK08].
On-Demand [MHAD15]. **Once** [MSE⁺17].
Online [ZCG18]. **Open** [AWD⁺18, Ano13h,
 Ano13i, ACG⁺07, ILG10, OK22, SKK22].
Open-Source
 [AWD⁺18, ILG10, OK22, SKK22].
OpenMDS [SKK22]. **Operand**
 [BHD09, MSI18]. **Operating** [AEJE17].
Operation [KCPG18, RAD⁺23].
Operations [JPC18]. **Opportunities**
 [RCK21, TNC19, Wu14]. **Opportunity**
 [MTH11]. **Optane** [MDSG20]. **Optical**
 [CGY⁺14]. **Optimal**
 [BHY⁺19, CFM⁺03, NMS14].
Optimization [ALKSA19, BHY⁺19,
 CNHH15, GO15, KDS22, LAS22, LLM⁺21,
 MMY⁺14, NR21, WCC14, YMG14, GD06].
Optimizations [BY17, WZLQ15, ZM07].
Optimized [EOA⁺23]. **Optimizing**
 [MSE⁺17]. **ORAM** [RM18]. **Orbital**
 [DL19]. **Orchestrating** [ASK⁺21]. **Order**
 [CTJ⁺17, DV13, Eec22, EHdSH20, HEDH21,
 IXS19, PGJ12, TOIS17, CMLV03].
Ordering [HR10]. **Organization**
 [AGK21, BSBD⁺08, GKKW07]. **OS-Level**
 [LKK19]. **Our** [FAR⁺23, Ano12k].
Out-Of-Order [DV13, IXS19, CTJ⁺17,
 HEDH21, TOIS17, CMLV03]. **Outcome**
 [CSSU20]. **Outputs** [WTSW21]. **Overall**
 [LX08]. **Overcoming** [HCK22]. **Overhead**
 [BGL⁺23, FBN⁺24, RM18, SRS20].
Overheads [KQGS16, SHK15, ZKH⁺20].
Overview [FUWT12].

Packet [KPKK20, MJB11]. **Packets**
 [FHL⁺10]. **Page**
 [LMK06, TV02, WMZY17, ZKH⁺20].
Page-based [LMK06]. **Page-Level** [TV02].
Pages [JLA16]. **Paging** [HBL⁺10].

Pairwise [GBS⁺20]. **Pairwise-Correlating** [GBS⁺20]. **Paradigm** [MKD⁺23, TASA13]. **Parallel** [ADS⁺19, AKK16, CLCG14, EHH21, KLZ12, KPEC10, LX08, MPPS17, XL07, AD06]. **Parallel/Distributed** [AKK16]. **Parallelism** [CF24, KHS⁺24b, yPSS⁺10, TMSA16, VE18]. **Parallelization** [DM06]. **Parity** [JSDK13]. **ParMiBench** [ILG10]. **Partially** [RL08]. **Partially-Minimal** [RL08]. **Partitioned** [JKK⁺21]. **Partitioning** [JLRA18, MCRV07]. **Party** [OSH16]. **Pass** [ZL18b]. **Passing** [GGM⁺16]. **PATer** [LCW⁺16]. **Path** [GKK⁺22, TOIS17]. **Paths** [RL17]. **Pattern** [Ano14c, Ano14d, CYAW20, SRS20, SHJW21, WSVS22]. **Patterns** [LPK16, WTSW21]. **PCIe** [LSJ⁺19]. **PCM** [KL18, WMZY17, YYK⁺18]. **PCM-Based** [KL18]. **pd** [AKK16]. **pd-gem5** [AKK16]. **Per-Core** [LMT⁺09, SW16]. **Per-task** [LJM⁺14]. **Performance** [AW15, ABC⁺19, BSD⁺19, BREM08, CCWY17, CZYY11, CLCG14, CTL⁺20, CFM⁺03, DPC16, DVAE18, EE14, FHL⁺10, GMMC15, GGS19, GF16, GSG⁺17, JSDK13, KKL⁺15, KKP⁺18, KH18, KWB⁺20, LKL⁺21, LTL23, MA19, MTH11, MDSG20, MWK⁺06, NK22, PLK⁺23, PL10, RMMLK16, RCS15, RB14, SKK22, SJM02, SJA⁺17, SCL06, SHJW21, TASA13, VP16, WCZ⁺12, WMJM23, YMBA19, YNS⁺08, YP23, ZVYW03, ZNTJE23, ZCG18, ZL18b, ZWT22, LHWB10, SYC14, Zho06]. **Performance-Efficient** [ZL18b]. **Performance-Energy** [KKL⁺15]. **Periodic** [GJ21]. **Peripheral** [AMW15]. **Permanent** [OKS⁺15, SKS⁺15]. **Persistence** [KQGS16, MAT17, PDGV16]. **Persistent** [KQGS16, MDSG20, WYL⁺15]. **Personalized** [KLR24]. **Perspective** [ILNS20, ZWT22]. **Petabyte** [Jac16a]. **PetaFLOP** [Jac16a]. **Phase** [Jun17, KJS⁺19, KHS⁺24b, KMJ18, KKL⁺07, Sez10]. **Phase-Change** [KJS⁺19]. **Phase-Level** [KHS⁺24b]. **Physical** [KWB⁺20, Rot08]. **Picture** [WXZ⁺21]. **PID** [RCS15]. **PID-Controlled** [RCS15]. **PIM** [CPK⁺23, NSC20, RCK21, SHJW21, ZTRA22]. **PIM-Based** [NSC20]. **PIM-GraphSCC** [NSC20]. **PIMSim** [XCW⁺19]. **Pipeline** [AS18, CTL⁺20, MSA19, PL15]. **Pipelined** [PLL08]. **Pipelining** [FUWT12]. **Pitfalls** [SQ23]. **Placement** [CKA20, HCM10, LLPC19]. **Plane** [TMSA16]. **Plane-Level** [TMSA16]. **Platform** [EGWM14]. **Platforms** [GO15, KDS22]. **Point** [ACSV02, DKD07, GF16, HLR21, LTL23]. **Pointer** [KKL⁺23, MAT17, RADZ19]. **Pointer-Based** [MAT17]. **Points** [AEJE17]. **Policies** [NPBS23]. **Policy** [JTG23, LLKS12, TMSA16, VGMSLN⁺18]. **Portable** [LJ18]. **Post** [KCB⁺20]. **Post-Silicon** [KCB⁺20]. **Potential** [CPK⁺23, LLKS12]. **Power** [AEJE17, ÇTNL16, CVP12, CGY⁺14, CLJ⁺02, DRGA12, DL20, FHL⁺10, GFAHSA24, KWL13, KPCK20, KWKK18, KG10, KFJ⁺03, LKK19, LMT⁺09, LLS⁺15, PGR⁺23, PHBC18, PP12, SKA⁺20, SBVB17, SKTC05, SW16, SSS⁺21, SPJ02, SCF04, SFFG⁺19, TVB⁺13, UKM02, WCK08, YHM17, YFPF14, ZAK⁺17, ZL18b, LHWB10, MWK⁺06]. **Power-Aware** [DL20, UKM02]. **Power-Efficient** [YHM17, SPJ02]. **Power-Gating** [ÇTNL16, ZL18b]. **Power-Limited** [AEJE17]. **POWER8** [LCW⁺16]. **pPIM** [SCB⁺20]. **PPT** [ABC⁺19]. **PQC** [LAM⁺22]. **Practical** [DPP23, DM06]. **PRAM** [JP13]. **Pre** [BGZT22, CSSU20, HKO⁺22, KHS⁺24a, MKSP05, VRFT24, WB14]. **Pre-Alignment** [HKO⁺22, KHS⁺24a]. **Pre-Executed** [MKSP05, WB14].

Pre-Execution [CSSU20]. **Pre-RTL** [VRFT24]. **Pre-Silicon** [BGZT22]. **Precise** [NFAE19]. **Precision** [NHKR19, SCB⁺20]. **Precision-Scaling** [SCB⁺20]. **Predication** [JMKP07, JMKP08]. **Predictability** [MXS19]. **Predicting** [PB16]. **Prediction** [CST⁺04, DVAE18, EF07, GAH⁺23, JJP⁺22, MLC24, MHAD15, PGJ12, PB16, PS17, SJ22, SYC07, SLKD14, SW19, YHY⁺22, YP23, ZCG18]. **Predictive** [WCYC09]. **predictor** [RZ06]. **Predictors** [ST20, SYC07]. **Prefetch** [PB16]. **Prefetcher** [BLKSA17, RJ20, YYK⁺18]. **Prefetchers** [JE22, PB16]. **Prefetching** [AGJ18, CSSU20, GBS⁺20, ILNS20, JTG23, KP21, LCW⁺16, PGJ12, TLG⁺11, ZMC17]. **PreGNN** [GKK⁺22]. **Preprocessing** [GKK⁺22, KLR24, YYK⁺18]. **Presence** [JTG23]. **Preserving** [MTM18]. **Pressure** [HCM10]. **Pressure-Aware** [HCM10]. **Prevent** [BBZ⁺19, LLSA18]. **Preventing** [LKP⁺23]. **Primate** [MHM⁺24]. **Priority** [LSJ⁺19, SK21]. **Priority-Based** [LSJ⁺19]. **Privacy** [MS16, MTM18]. **Privacy-Preserving** [MTM18]. **Proactive** [FJ08]. **Probabilistic** [EF07, RZ06]. **Probability** [IKW⁺20]. **Probability-Based** [IKW⁺20]. **Problem** [HS04]. **Proceedings** [Ano10g]. **Process** [DOM⁺07, DOM⁺08, MTT12, Mus09, ZZJ18]. **Process-in-Memory** [ZZJ18]. **Process-Variation** [Mus09]. **Processing** [AG17, AA19, AWD⁺18, BHL⁺18, BGP⁺17, CTJ⁺17, CHK⁺18, FSO⁺22, FFAMK15, HCK⁺21, HKO⁺22, JPC18, KPKK20, KZL18, LQYF23, NSC20, SRV⁺19, SRS20, ST20, SPHS22, SKS⁺24, XGH⁺22, XCW⁺19, YQL⁺24, YLK21, YKP⁺22, ZZW⁺22, ZTRA22]. **Processing-in** [JPC18]. **Processing-in-DRAM** [ZTRA22]. **Processing-In-Memory** [YLK21, BGP⁺17, SPHS22, XCW⁺19]. **Processor** [BDBS⁺08, CZYY11, KPEC10, KFJ⁺03, LCW⁺16, LJ04, MKSP05, SCB⁺20, VE18, YKMG15]. **Processor-in-Memory** [SCB⁺20]. **Processors** [ADS⁺19, ASK⁺21, ACSV02, CXS18, FJ08, GGS19, GMM⁺19, HEDH21, LLPC19, LMC⁺09, MHM⁺24, Mus09, NK22, PGJ12, RADZ19, RYSN04, SRH20, SMY15, TOIS17, TDO16, VS11, WCYC09, WB14, CMLV03, Zho06]. **Production** [MKD⁺23]. **Profiles** [CNHH15]. **Profiling** [CV15, GMMC15, SFFG⁺19]. **Program** [KKL⁺07, NGS15, SSTS17, SHK15]. **Programmable** [DCG12, DEC⁺18, SCB⁺20]. **Programming** [KLKK14, MKD⁺23, QYZ⁺24]. **Programs** [GRCV02, MPPS17, ORS⁺06]. **Progress** [NB24]. **Progressive** [AG17]. **Promotion** [JTG23, MDK⁺23]. **Proposed** [BGS⁺20]. **Protection** [OK22, Vol21]. **Protocol** [KSB19]. **Providing** [KKH14]. **PRR** [SKD09]. **Pruned** [WTSW21]. **Pruning** [AQ24]. **Publication** [Ano11j]. **Publishing** [Ano12c, Ano13h, Ano13i]. **Pulley** [LAS22]. **Purpose** [DPP23, WSVS22].

Q [GMM⁺19]. **Q-Learning** [GMM⁺19]. **QAOA** [UTT⁺24]. **Quality** [YC15]. **Quantifying** [TND⁺21]. **Quantitative** [KPPK21, LPK16]. **Quantization** [SBQK21]. **Quantum** [AS18, AQ24, EOA⁺23, RTKQ21, RK22, TXD⁺23, ZB19]. **Quantum-Dot** [AS18]. **Quasi** [JDK⁺02]. **Quasi-Static** [JDK⁺02]. **Qubit** [EOA⁺23]. **quick** [Ano12k].

R.I.P. [Eec24]. **Race** [EGWM14]. **Racetrack** [HKO⁺22, KHB⁺19, KHS⁺24a]. **Radar** [WLL⁺22]. **Radix** [SD04, SCL13]. **RAM** [JP13, MVJ17, SSVS21, YFPF14]. **RAMBO** [LLM⁺21]. **Ramulator** [KYM16, LTB⁺24]. **Random** [RL09, SKS⁺24]. **Randomization** [BGS⁺20]. **Randomized** [KYP21, RL08]. **Randomness** [TS24]. **Ransomware**

[MPA⁺18]. **Rapid** [DVAE18, SRS11]. **RAS** [GLJ⁺21, RCS15]. **Rate** [PL10]. **Rate-Based** [PL10]. **ray** [NBW⁺23]. **Re** [RASW19]. **Re-Routing** [RASW19]. **Reach** [AQ24]. **Read** [MVJ17, MSE⁺17, ZZJ18]. **Read-Disturbance** [MVJ17]. **Read-Once** [MSE⁺17]. **Reads** [KHS⁺24a]. **Real** [PPG⁺17, RSO21]. **Real-Time** [PPG⁺17, RSO21]. **Rebasing** [ILNS20]. **Rebuttal** [BREM08]. **Recommendation** [KLR24, LQYF23]. **Reconfigurable** [AFG⁺24, LAX⁺20, LLD⁺18, LYL⁺16, SSSM18, TNC19, WLL⁺22, ZL18a]. **Recovery** [EHdSH20, MPA⁺18, MAT17]. **Redistribution** [LHPR23]. **ReDRAM** [SSSM18]. **Reduce** [Cit04, KG10]. **Reducing** [FHL⁺10, FBN⁺24, KWL13, KQGS16, KJK21, Zha06]. **Reduction** [AYL22, HLH16, KKKH18, KPL⁺21, KFJ⁺03, Per21, SCF04, UTT⁺24]. **Redundancy** [GWR08]. **Redundant** [WLZZ23]. **Refactored** [LKA15]. **reference** [Rot08]. **Refresh** [KKKH18, LLSA18]. **Refuting** [BGS⁺20]. **Regional** [YJZ15]. **Register** [BSBD⁺08, EE16, JEAG⁺19, Rot08]. **Registers** [BHD09]. **Regression** [YYK⁺18]. **Regulation** [HPS23]. **Reinforcement** [JE22, KHS⁺24b]. **Relaxed** [PTND24]. **Reliability** [AQ24, ÇE14, DD18, HSUS11, SMY15, TMNK19]. **Reliable** [KMJ18, KKL⁺07]. **Relocation** [SKD09]. **Remapping** [WMZY17]. **Remote** [KSB19]. **Removing** [ZKH⁺20]. **Reorder** [ASSK21]. **Reordering** [MNFI20, SJM02, ZZW⁺22]. **Replacement** [NPBS23, VGMSLN⁺18]. **Replication** [Vol21]. **Replication-Aware** [Vol21]. **Reporting** [SRS20]. **Representation** [NGS15, WXZ⁺21]. **Request** [SJM02]. **ReRAM** [LHZ19]. **ReRAM-Based** [LHZ19]. **ReRAMs** [ZZJ18]. **Resampling** [PL10]. **Research** [AWD⁺18, KL02]. **Reservation** [LZS⁺08]. **Resilience** [GLJ⁺21, LBB⁺19, OKS⁺15, SKS⁺15, SHK15]. **Resiliency** [LLS⁺15]. **Resilient** [ODKK18]. **Resistive** [MLA⁺14, YKMG15, YWG17, ZL17]. **Resource** [KCP⁺19, KQD18, LZS⁺08, LLM⁺21, ODKK18, RMMLK16, SJ22, CMLV03]. **resource-conscious** [CMLV03]. **Resource-Scalable** [SJ22]. **Response** [EHH21, FHL⁺10]. **Restating** [EE14]. **Results** [ACSV02, MKSP05, WB14]. **RETROFIT** [ZKF⁺18]. **Reusable** [JLKK23]. **Reuse** [BY17, CMP⁺14, LPK16, YHM17]. **Reusing** [MKSP05]. **Revenues** [DOM⁺07, DOM⁺08]. **Reviewers** [Ano11b, Ano12b, Ano13b]. **Revisiting** [WB14, ZWT22]. **Rich** [LBB⁺19]. **Ring** [LAM⁺22]. **Ring-LWE** [LAM⁺22]. **RIO** [HEDH21]. **RISC** [LCW⁺24, ZBA⁺20]. **RISC-V** [LCW⁺24, ZBA⁺20]. **ROB** [HEDH21]. **ROB-Centric** [HEDH21]. **Robotics** [KHS⁺24b]. **Rock** [Ano15h, Ano15i]. **Rollback** [MAT17]. **Rollback-Recovery** [MAT17]. **Roofline** [IPS14]. **Router** [KWL13, PL15, SRLP09, ZL18b]. **RouteReplies** [ZZW⁺23]. **Routing** [FD08, GDF⁺04, GF16, KK21, KL18, MCKW10, RL08, RL09, RASW19, SDTG04, SCF04, SCL13, TD02, XYZ15]. **Row** [KNQ15, KLCA21, LLSA18, LKP⁺23, SJM17]. **Row-Hammering** [LLSA18]. **Row-Streaming** [KLCA21]. **Rowhammer** [FBN⁺24, ZTRA22]. **RPCs** [LAX⁺20]. **RPPM** [DVAE18]. **RTL** [VRFT24]. **RTSim** [KHB⁺19]. **Run** [KNGK15, LX08, RADZ19]. **Run-Time** [KNGK15, RADZ19, LX08]. **Runahead** [GBS⁺20, MKSP05, NFAE19, WB14]. **Runtime** [GMMC15, MPPS17, MKD⁺23, MXS19, SPHS22, ZB19]. **Runtime-Assisted** [MPPS17]. **Rusty** [MXS19]. **s** [Jac16a]. **SA** [SHW19]. **Safe**

[MLK15, MKP⁺24]. **Safer** [FAR⁺23]. **Safety** [ODKK18]. **Safety-Critical** [ODKK18]. **SALAD** [SCR⁺17]. **Sampled** [LJ04]. **Scalability** [VP16, MWK⁺06]. **Scalable** [APK⁺18, ABC⁺19, FSO⁺22, GWR08, JJP⁺22, KKL20, KKJ⁺22, MGH⁺22, MCY⁺12, RSRT19, SRV⁺19, SJ22, SSS⁺21, TASA13, ZL18b]. **Scale** [AG17, DRGA12, DSVK12, GLJ⁺21, HCM10, LKR21, LHE⁺21, MTH11, MKD⁺23]. **Scale-Model** [LHE⁺21]. **Scale-Out** [MKD⁺23]. **Scaled** [ILXY18a, ILXY18b, KCPG18]. **ScaleGPU** [KLKK14]. **Scaling** [CTNL16, DL20, GO15, MLM⁺06, MKP⁺24, SPJ02, SCF04, SCB⁺20, YC15]. **Scatter** [SKS⁺24]. **SCC** [CLCG14]. **SCEPTER** [DPC16]. **Sched** [NPS21]. **Scheduling** [APK⁺21, BRUS21, CCWY17, DK16, DC18, LLKS12, LKKS15, LA16, LSJ⁺19, MNU⁺15, SBVB17, SK21]. **Scheme** [CLCG14, MMR17, SLC03, WJFH11]. **Scientists** [GMPMC⁺23]. **Second** [LMJ12]. **Section** [MNU⁺15]. **Section-Aware** [MNU⁺15]. **Secure** [KZY⁺19, NK22, ODKK18, Sez10, SM18, TWI⁺24]. **Security** [BGZT22, BGS⁺20, DK16, HPS23, HSUS11, HBW⁺23, KZY⁺19, NK22, OSH16, PGC22, TS24, Ano16d]. **Selection** [NR21]. **Selective** [DV13, MVJ17]. **Self** [LHPR23, ZTRA22]. **Self-Attention** [LHPR23]. **Self-Tracking** [ZTRA22]. **semantics** [BLM06]. **Semi** [MAHK18]. **Semi-Coherent** [MAHK18]. **SEMS** [KKJ⁺22]. **Sensing** [HDAS18]. **Sensitive** [RYSN04]. **Sensitivity** [NPBS23]. **Sequence** [SJS24, VRS18]. **Sequencing** [LJ18]. **sequential** [ORS⁺06]. **Serial** [JAM17, WSVS22]. **Server** [ADS⁺19, ASK⁺21, TMNK19, WLL17]. **Servers** [JSLW20, KPCK20, PHBC18]. **Service** [KYP21, NK22, YC15]. **Service-Aware** [YC15]. **Services** [Ano10g, Ano12c]. **Set** [GIH⁺24, MMR17, RAD⁺23, YJZ15]. **Set-Granular** [YJZ15]. **Shader** [WCYC09]. **Shaping** [JLRA18]. **Shared** [CZYY11, FJ08, IXS18, SLKD14, SRLP09]. **Shared-Buffer** [SRLP09]. **Shared-Memory** [IXS18]. **Sharing** [GG17, KCP⁺19, LMJ12, RMMLK16, WYM⁺16]. **Shell** [SKK22]. **Shifting** [TVB⁺13]. **Shimmer** [TMNK19]. **Shutdown** [PHBC18]. **Short** [GWR08, ZZJ18]. **Should** [ZKW12]. **Shrink** [LWB13]. **Shrink-Fit** [LWB13]. **Shuffle** [WCZ⁺12]. **Shutdown** [WCYC09]. **Side** [MLC24, MKMJ23]. **Side-Channel** [MLC24]. **Side-Channels** [MKMJ23]. **Sifting** [AEJE17]. **Silicon** [BGZT22, CMP⁺14, DXSS15, FBN⁺24, KCB⁺20]. **Sim** [XGH⁺22]. **SIMD** [WCZ⁺12]. **Simple** [NPS21]. **SimpleSSD** [JZA⁺18]. **Simplified** [BSMB23]. **SIMT** [LPK16]. **Simulating** [FAR⁺23]. **Simulation** [AKK16, ACG⁺07, DM06, FAR⁺23, Hos18, JZA⁺18, KL02, LHZ19, LHE⁺21, LJ04, MMAAK21, VRFT24, SCL06]. **Simulation-Based** [KL02]. **Simulator** [Ano10a, FLSZ17, GLH⁺20, JC17, KHB⁺19, KYM16, LHCK22, LYR⁺20, LTB⁺24, MGHP20, OK22, PZX15, PHO⁺15, RCBJ11, XGH⁺22, XCW⁺19, YLK21]. **Simulators** [BVL09, CAPS09, EHH21]. **Simultaneous** [SHW19, WYM⁺16]. **Single** [BEA⁺13, KKL⁺15, KH18, KFJ⁺03, MNU⁺15, MJBD11, SD02]. **Single-Cycle** [MJBD11]. **Single-ISA** [KFJ⁺03, MNU⁺15]. **Single-Thread** [KH18]. **Singular** [LCKA23]. **Singular-Value** [LCKA23]. **Situ** [MNFI20]. **Size** [NMS14]. **Sizing** [LWB13]. **Sky** [KWB⁺20]. **Slicing** [YSL⁺21]. **Slowdown** [SJ22, ZCG18]. **Small** [JLA16, NB24]. **SmaQ** [SBQK21]. **Smart** [MGH⁺22, RMM24, SBQK21]. **SmartIndex** [WMJM23]. **SmartSSD** [LZL⁺20]. **SMT** [HR10, KH18, RYSN04, SHW19, TVB⁺13]. **SMT-Directory** [HR10]. **SMT-SA**

[SHW19]. **SoC** [HBW⁺23, MMY⁺14]. **Society** [Ano09a, Ano10c, Ano11i, Ano08c, Ano09l, Ano09m, Ano10f, Ano10l, Ano10a, Ano10n, Ano10m, Ano11i, Ano12j, Ano13j, Ano14e, Ano14f, Ano15f, Ano15g]. **Socket** [PGC22, SPAP10]. **SoCs** [APK⁺21, BHY⁺19, SKA⁺20]. **SoCurity** [HBW⁺23]. **Soft** [EE16, EUVG06, KRB⁺13, MHM⁺24, PL15, SG14, YE07]. **Software** [BKA⁺09, CTJ⁺17, CV15, FAR⁺23, GAH⁺23, LMK06, MKM17, TVB⁺13, XWG⁺14]. **Solid** [JZA⁺18, KKL20, SYC14, YNS⁺08]. **Solid-State** [KKL20, SYC14]. **Solution** [SAA⁺23]. **Sorting** [LCHL20, LAS22]. **Source** [AWD⁺18, ILG10, OK22, SKK22]. **Space** [DL19, LLPC19]. **Sparing** [MCM13]. **Sparse** [LWM20, LZD⁺23, YG18]. **SparseLeakyNets** [MLC24]. **Sparsity** [MLC24, MNF120, PTND24]. **Sparsity-Aware** [MLC24]. **Spatial** [SW19, WLDN19, ZCG18]. **SPEC** [KL02]. **Special** [Ano10e]. **Specialization** [NGS15]. **Specialized** [ST20]. **Specific** [BSD⁺19, WCC14]. **Spectre** [LG20]. **Speculation** [ASSK21, MGI14, RL17, XJ09, YHY⁺22]. **Speculative** [ASSK21, BBZ⁺19, GQLZ19, PJ22, Per21, SLC03]. **Speed** [MTT12, MCRV07, ZL18a]. **Speeding** [RASW19]. **Speedup** [Eec24, LJ04]. **Spintronics** [CHK⁺18, LJ18]. **Spintronics-Based** [LJ18]. **SPMD** [GG11]. **SRAM** [GIH⁺24, MV15, SRS20]. **SSD** [APK⁺18, BGL⁺23, KKP⁺18, KJK21, LGLK17, LZL⁺20, LKL⁺21, LHCK22, MPA⁺18, PLK⁺23, TASA13]. **SSDs** [IKW⁺20, KLWJ21, LKKS15, yPSS⁺10, TASA13, TMSA16]. **SSE** [NK22]. **Stack** [HCK22, KLWJ21, LEBM20, MKD⁺23, YLK21, ZKH⁺20]. **Stacked** [RMM24, SFFG⁺19]. **Stacking** [HRF⁺11]. **Stacks** [EHDH18, KNGK15]. **Stage** [EHDH18, NBH13]. **Stars** [Ano15h, Ano15i]. **State** [JZA⁺18, KKL20, SYC14, YNS⁺08, ZAK⁺17]. **Static** [FUWT12, JDK⁺02]. **Statistical** [JLRA18, KCPG18, MS16]. **Stay** [Ano10f, Ano13j, GBK⁺09]. **Steroids** [JLA16]. **Stochastic** [KNG⁺18, Man15, SJS24]. **STONNE** [MMAAK21]. **Storage** [AGK21, DSVK12, JKK⁺21, LKA15, LZL⁺20, PS17, WZLQ15, ZKH⁺20]. **Storage-Effective** [AGK21]. **Storage-Free** [PS17]. **Store** [LHWB10, PJ22]. **Stores** [HS04, KKLL22]. **Strategy** [HCM10, NPS21]. **Stream** [KPEC10, MM03, WLN22]. **Stream-Based** [MM03]. **Streaming** [CSSU20, KLCA21, KLZ12]. **Streamlining** [YQL⁺24]. **Strength** [Per21, RK22]. **Strict** [SJM02]. **Stride** [YHY⁺22]. **String** [PLL08]. **Stripes** [JAM17]. **Structure** [CLJ⁺02, KLCA21, NBW⁺23, SSTS17, SJM17]. **Structured** [AYL22, LWM20, PTND24]. **Structured-Sparse** [LWM20]. **Structures** [NSC20]. **STT** [ILXY18a, ILXY18b, JP13, MVJ17, SSVS21, YPFP14, ZBA⁺20]. **STT-MRAM** [ILXY18a, ILXY18b, ZBA⁺20]. **STT-RAM** [YPFP14]. **STT-RAM-Based** [SSVS21]. **Student** [Ano10e]. **Studies** [DSVK12]. **Study** [CKA20, KKLL22, NMS14]. **Studying** [ZTS16]. **Sub** [GGM⁺16]. **Sub-System** [GGM⁺16]. **subarray** [Zha06]. **Subtleties** [BLM06, KNGK15]. **Sufficient** [XYZ15]. **Suite** [MTM18, WLL17]. **Super** [WMZY17]. **Super-Dense** [WMZY17]. **Superscalar** [VE18]. **Supply** [KLZ12, MTT12]. **Support** [DKD07, GMMC15, KNQ15, MLK15, MKM17, MSI18, MKP⁺24, SPS22]. **Supporting** [GIH⁺24, NSF⁺18, PTND24, SRS11]. **Survive** [MAT17]. **Sustainability** [Eec22, ZNTJE23]. **Sustainable** [Wu14]. **SVSoC** [GQLZ19]. **SW** [DCG12]. **Switch** [DC18, TVB⁺13]. **Switched** [JLP07].

Switching [SRH20]. **Symmetric** [SCR⁺17]. **Synchronization** [LLD⁺18, SLC03]. **Synchronous** [LKKS15]. **Synctium** [KPEC10]. **System** [GGM⁺16, Jac16a, JZA⁺18, KNG⁺18, KL18, KKJ⁺22, KSO⁺16, KLZ12, KR18, LQYF23, MXS19, RCBJ11, SJA⁺17, TS24, WLL⁺22, XL07, ZLS10, ZBA⁺20, LLLM06]. **System-on-a-Chip** [XL07]. **Systems** [AKK16, BDBS⁺08, CWK⁺22, CKA20, CLJ⁺02, CEA18, GQLZ19, GJ21, GDU⁺24, GRCV02, HBL⁺10, HH22, ILG10, KJS⁺19, KLR24, LLJK23, LBB⁺19, LSJ⁺19, LJM⁺14, MGH⁺22, MAHK18, PPG⁺17, PL15, PZX15, PPG11, SLC03, SPAP10, TLG⁺11, ZVYW03, LHWB10]. **Systems-on-a-Chip** [GQLZ19]. **Systolic** [KLCA21, LWM20, SHW19].

T [LLJK23]. **T-CAT** [LLJK23]. **Table** [Ano14g, Ano14h, Ano15j, Ano15k, Ano16p, Ano16n, Ano16o, KL18, Ano12h]. **Tackling** [RCS15]. **tag** [YE07]. **tag-match** [YE07]. **Tagging** [KKL⁺23]. **Tail** [RSO21]. **Tails** [SSTS17]. **Take** [GKK⁺22]. **Tale** [FAR⁺23]. **Tangible** [SMLS15]. **Targeting** [KDS22]. **Task** [KLZ12, MPPS17, SK21, LJM⁺14]. **Task-Based** [MPPS17]. **Task-Parallel** [KLZ12]. **TB** [Jac16a]. **TB/s** [Jac16a]. **TBM** [TMSA16]. **Technique** [AMW15, ILXY18a, KRB⁺13, MV15, Mus09, WCYC09]. **Techniques** [JDK⁺02, PL10, SSVS21]. **Technology** [GLH⁺20]. **TeleVM** [LCW⁺24]. **Temperature** [UTT⁺24]. **Temporal** [BLKSA17, EF07]. **Tenant** [LSJ⁺19]. **Tensor** [KPL⁺21, LWM20]. **TERMinator** [MTM18]. **Theoretic** [PPA⁺24]. **There** [Ano12k]. **Thermal** [CFM⁺03, LYR⁺20, Mic20, SRS11, Wu14]. **Thermal-Capable** [LYR⁺20]. **Thermally** [XYMY16]. **Thinking** [Ano16k]. **Third** [OSH16]. **Third-Party** [OSH16]. **Thread** [CCWY17, GBK⁺09, KKL⁺15, KH18, MNU⁺15, MGI14, MKP⁺24, NPS21, RYSN04, SLKD14]. **Thread-Level** [MGI14]. **Thread-Safe** [MKP⁺24]. **Thread-Sensitive** [RYSN04]. **Threaded** [VS11]. **Threading** [SMZ18]. **Threads** [HLH16, MKM17, ORS⁺06]. **Threats** [CWK⁺22]. **Three** [RL08]. **Three-Dimensional** [RL08]. **Threshold** [KPEC10]. **Throttling** [UKM02]. **Throughput** [ILXY18a, ILXY18b, KKK13, LLPC19, MSA19, Mic13, SRLP09, SCL13]. **Tiered** [CKA20, LLJK23, MDK⁺23]. **Tile** [Mus09, YSL⁺21, CZYY11]. **Tile-Based** [Mus09]. **Tiled** [LCKA23]. **Tilera** [CZYY11]. **Time** [CVF⁺24, Eec24, KNGK15, LLSA18, PPG⁺17, RADZ19, RSO21, LX08]. **Timing** [BGS⁺20, EHH21, MLC24, RL17, XJ09]. **TLB** [CLJ⁺02, PHBC18]. **Toggle** [PBO⁺15]. **Toggle-Aware** [PBO⁺15]. **TokenSmart** [SSS⁺21]. **Tolerance** [EUVG06, Zho06]. **Tolerant** [GDF⁺04, HRF⁺11, PL15]. **Toolchain** [VRFT24]. **Topology** [GD06, KBD07]. **Tori** [GDF⁺04, SDTG04]. **Torus** [RL09]. **Trace** [MM03]. **Traces** [PV06]. **Tracking** [ZTRA22]. **Trade** [BSD⁺19]. **Trade-offs** [BSD⁺19]. **Tradeoff** [SHK15]. **Traffic** [HLH16, JLRA18, TD02, ZLAE17]. **Train** [CVF⁺24]. **Train-Time** [CVF⁺24]. **Training** [JKK⁺21, KR18, LKR21, LHZ19, MGH⁺22, SBQK21, YP23]. **Transaction** [GLH⁺20, LZS⁺08]. **Transaction-Aware** [LZS⁺08]. **Transaction-Command** [GLH⁺20]. **Transactional** [BKA⁺09, DD18, LLD⁺18, WJFH11, WYL⁺15, XWG⁺14, BLM06]. **Transactions** [Ano10b, Ano14c, Ano14d, NB24, Ano12k, Ano13e]. **Transcending** [CTJ⁺17]. **Transfer** [RMA⁺20]. **Transformation** [KKKH18, VD02]. **Transformer** [CPK⁺23, LCKA23]. **Transformer-Based** [CPK⁺23, LCKA23]. **Transforms** [PPA⁺24]. **Transient**

[BBZ⁺19]. **Transients** [Mic20]. **Translation** [IKW⁺20, LMJ12, LLLM06]. **Translation-Lookaside** [LMJ12]. **Transparent** [KKH14, WLN22]. **Tree** [JLKK23, PJ22, SJM17, TWI⁺24, Ant09, GVG⁺08]. **Tree-Based** [PJ22]. **Trees** [SB18]. **TRiM** [KPL⁺21]. **Trojan** [CWK⁺22]. **Trusted** [TXD⁺23]. **TrustZone** [PPG⁺17]. **TrustZone-Assisted** [PPG⁺17]. **Tulip** [GFAHSA24]. **TUNE** [CXS18]. **Tuner** [LCW⁺16]. **Tuning** [CXS18, YMBA19]. **Turbo** [Mic20, VMS17]. **Turn** [GFAHSA24]. **Turn-Free** [GFAHSA24]. **TWiCe** [LLSA18]. **Twin** [TMSA16]. **TWL** [KJS⁺19]. **Two** [LCHL20]. **Two-Directional** [LCHL20].

UDIR [AFG⁺24]. **Ultra** [MTT12]. **Ultra-low** [MTT12]. **Unaware** [KLKK14]. **Understanding** [HXL⁺22, LKR21, WYY⁺23, XHG⁺19, YCD⁺20, ZYZ⁺22]. **Unexpected** [MDSG20]. **Unfairness** [SJA⁺17]. **Unidirectional** [Ant09, GVG⁺08]. **Unification** [RB14]. **Unified** [AFG⁺24, LHZ19]. **UNISIM** [ACG⁺07]. **Unit** [DCG12, GG17]. **Units** [GMMC15, JLRA18, MTT12]. **Unleashing** [CPK⁺23]. **Untitled** [Ska09b, Ska10b, Ska11b]. **Unused** [KG10]. **updates** [RZ06]. **Upgrading** [IPS14]. **Ups** [MCRV07]. **Use** [Eec24, FJ08, YSL⁺21]. **Useful** [GMPMC⁺23]. **Usefulness** [PB16]. **User** [MLM⁺06, PZX15, LLLM06]. **User-Driven** [MLM⁺06]. **User-Friendly** [PZX15]. **user-level** [LLLM06]. **Using** [AG17, BHY⁺19, CHK⁺18, GGS19, GO15, HKO⁺22, KHS⁺24a, KDL23, KKP⁺18, KCP⁺19, KLCA21, KH18, LMT⁺09, LLM⁺21, LJ04, MLC24, MCY⁺12, NSC20, PL10, RADZ19, RAD⁺23, SK21, WLWZ19, WB14, WTSW21, YE07, YHM17, BREM08, JDK⁺02, MTT12, SLC03, SCL06, Zho06]. **Utilization** [MA19, TMSA16].

V [LCW⁺24, ZBA⁺20]. **Validation** [GWR08, VRFT24]. **Valley** [GBK⁺09]. **Value** [AS14, CST⁺04, KKKH18, KLL22, LCKA23, PLK⁺23, SBQK21, SW19, SRLM20, YHY⁺22]. **Value-Aware** [AS14]. **Values** [EUVG06, KRB⁺13]. **Variability** [DRGA12, RCS15]. **Variable** [RK22]. **Variation** [MTT12, Mus09]. **Variations** [DOM⁺07, DOM⁺08]. **Variety** [AG17]. **vCache** [KKH14]. **Vector** [GIH⁺24]. **Vehicles** [APK⁺21]. **Verification** [ZLS10]. **Versatile** [LTL23, WZLQ15]. **Vertical** [HRF⁺11, ILXY18b]. **Via** [KFJ⁺03, BY17, CCWY17, KHS⁺24b, LYY⁺21, YMBA19]. **Victimization** [ZKH⁺20]. **View** [KKH14]. **Virtual** [ÇE14, GIH⁺24, KNGK15, LCW⁺24, PHBC18]. **Virtualization** [SYC14]. **Virtualized** [HBL⁺10, KKH14]. **Vision** [GQLZ19]. **Visual** [KWB⁺20]. **VLIW** [Jac16b]. **VMOR** [MSI18]. **Vol** [Ano15a, Ano16a, Ano16b, Ano17, Ano18, Ano19, Ano20, Ano21, Ano22]. **Volatile** [LKR21, PZX15, RM18, SM18, VHN15, WZLQ15]. **Voltage** [ÇTNL16, CKZ⁺20, HDAS18, KCPG18, MTT12, SPJ02, SCF04, YC15]. **Voltages** [MTT12]. **vs** [GBK⁺09]. **Vulnerabilities** [BGZT22, HSUS11, KWKK18, KZY⁺19].

Wall [HCK22]. **Warehouse** [AG17, MTH11]. **Warehouse-Scale** [AG17, MTH11]. **Warp** [ZTS16]. **Way** [FAR⁺23, ZVYW03, Ano12k]. **Way-Halting** [ZVYW03]. **Wear** [KJS⁺19, LZLX15, ZKF⁺18]. **Wear-Leveling** [LZLX15]. **Wearables** [Ano15i]. **Web** [MGI14, VP16, ZSLR14]. **Webpage** [ZSLR14]. **Weight** [CVF⁺24, GG17, IXS19]. **Weight-Sharing** [GG17]. **Weighted** [EE14, RL09]. **Weighted-IPC** [EE14]. **Whole** [WXZ⁺21]. **Whole-Picture** [WXZ⁺21]. **Window** [LLSA18]. **Wire** [Cit04, ZL18a]. **Wire-Speed** [ZL18a]. **Wires** [TNC19].

Word [VD02]. **Word-Interleaving** [VD02]. **Words** [KG10]. **Work** [Eec24]. **Workers** [VP16]. **Workflows** [TMSX23]. **Worklist** [ZMC17]. **Worklist-Directed** [ZMC17]. **Workload** [BSD⁺19, EE14, KL02, SRH20, WXZ⁺21]. **Workload-Specific** [BSD⁺19]. **Workloads** [BHL⁺18, DS09, JLS⁺23, LMT⁺09, PKKK23, PLK⁺23, XHG⁺19, ZAK⁺17]. **Worst** [SKTC05, SCL13, TD02]. **Worst-Case** [SCL13, TD02]. **WPC** [WXZ⁺21]. **Write** [ILXY18a, LKKS15, WMZY17]. **Writes** [ILXY18b].

X [AGK21, NBW⁺23, XHG⁺19]. **X-ray** [NBW⁺23]. **Xilinx** [SKK22]. **XML** [BVL09]. **XML-Based** [BVL09].

Years [Ano10b]. **Yourself** [Ano10d].

Zebra [KKKH18]. **Zero** [BGL⁺23, KKKH18, KLWJ21]. **Zero-Aware** [KKKH18]. **Zero-Copying** [KLWJ21]. **Zero-Overhead** [BGL⁺23].

References

[AA19] Berkin Akin and Alaa R. Alameldeen. A case for asymmetric processing in memory. *IEEE Computer Architecture Letters*, 18(1):22–25, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

[ABC⁺19] Yehia Arafa, Abdel-Hameed A. Badawy, Gopinath Chen-nupati, Nandakishore Santhi, and Stephan Eidenbenz.

[ACG⁺07]

[ACSV02]

[AD06]

PPT-GPU: Scalable GPU performance modeling. *IEEE Computer Architecture Letters*, 18(1):55–58, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

August:2007:UOS

D. August, J. Chang, S. Girbal, D. Gracia-Perez, G. Mouchard, D. A. Penry, O. Temam, and N. Vachharajani. UNISIM: an open simulation environment and library for complex architecture design and collaborative development. *IEEE Computer Architecture Letters*, 6(2):45–48, February 2007. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Alvarez:2002:IRF

C. Alvarez, J. Corbal, E. Salami, and M. Valero. Initial results on fuzzy floating point computation for multimedia processors. *IEEE Computer Architecture Letters*, 1(1):1, January 2002. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Ahn:2006:DPA

Jung Ho Ahn and W. J. Dally. Data parallel address architecture. *IEEE Computer Architecture Letters*, 5(1):30–33, January 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [ADS⁺19] **Agrawal:2019:MPS**
 V. Agrawal, M. A. Dinani, Y. Shui, M. Ferdman, and N. Honarmand. Massively parallel server processors. *IEEE Computer Architecture Letters*, 18(1):75–78, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [AEJE17] **Adileh:2017:MPH**
 Almutaz Adileh, Stijn Eyerman, Aamer Jaleel, and Lieven Eeckhout. Mind the power holes: Sifting operating points in power-limited heterogeneous multicores. *IEEE Computer Architecture Letters*, 16(1):56–59, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [AFG⁺24] **Agarwal:2024:UTU**
 Nikhil Agarwal, Mitchell Fream, Souradip Ghosh, Brian C. Schwedock, and Nathan Beckmann. UDIR: Towards a unified compiler framework for reconfigurable dataflow architectures. *IEEE Computer Architecture Letters*, 23(1):99–103, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [AG17] **Ahmadvand:2017:UDV**
 Hossein Ahmadvand and Maziar Goudarzi. Using data variety for efficient progressive big data processing in warehouse-scale computers. *IEEE Computer Architecture Letters*, 16(2):166–169, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [AGJ18] **AlBarakat:2018:MFM**
 Laith M. AlBarakat, V. Paul Gratz, and Daniel A. Jiménez. MTB-Fetch: Multithreading aware hardware prefetching for chip multiprocessors. *IEEE Computer Architecture Letters*, 17(2):175–178, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [AGK21] **Asheim:2021:BXS**
 Truls Asheim, Boris Grot, and Rakesh Kumar. BTB-X: a storage-effective BTB organization. *IEEE Computer Architecture Letters*, 20(2):134–137, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [AKK16] **Alian:2016:PGS**
 Mohammad Alian, Daehoon Kim, and Nam Sung Kim. pdgem5: Simulation infrastructure for parallel/distributed computer systems. *IEEE Computer Architecture Letters*, 15(1):41–44, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [ALKSA19] **Ansari:2019:CLO** Ali Ansari, Pejman Lotfi-Kamran, and Hamid Sarbazi-Azad. Code layout optimization for near-ideal instruction cache. *IEEE Computer Architecture Letters*, 18(2):124–127, July 2019. ISSN 1556-6064. [Ano08b]
- [ALSJ09] **Ahn:2009:MDE** Jung Ho Ahn, Jacob Leverich, Robert S. Schreiber, and Norman P. Jouppi. Multicore DIMM: an energy efficient memory module with independently controlled DRAMs. *IEEE Computer Architecture Letters*, 8(1):5–8, January/June 2009. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic). [Ano08c]
- [AMW15] **Azriel:2015:PMT** Leonid Azriel, Avi Mendelson, and Uri Weiser. Peripheral memory: a technique for fighting memory bandwidth bottleneck. *IEEE Computer Architecture Letters*, 14(1):54–57, January/June 2015. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic). [Ano09a]
- [Ano08a] **Anonymous:2008:EBC** Anonymous. Editorial board [cover2]. *IEEE Computer Architecture Letters*, 7(2):c2, July 2008. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic). [Ano09b]
- Anonymous:2008:FC** Anonymous. [Front cover]. *IEEE Computer Architecture Letters*, 7(2):c1, July 2008. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Anonymous:2008:ICS** Anonymous. IEEE Computer Society [cover 4]. *IEEE Computer Architecture Letters*, 7(2):c4, July 2008. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Anonymous:2008:IA** Anonymous. Information for authors. *IEEE Computer Architecture Letters*, 7(2):c3, July 2008. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Anonymous:2009:AIC** Anonymous. Ad — IEEE Computer Society Digital Library. *IEEE Computer Architecture Letters*, 8(1):36, January/June 2009. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Anonymous:2009:Aa** Anonymous. [Advertisement]. *IEEE Computer Architecture Letters*, 8(1):35, January/June 2009. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [Ano09c] **Anonymous:2009:Ab** Anonymous. [Advertisement]. *IEEE Computer Architecture Letters*, 8(2):68, July/December 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano09d] **Anonymous:2009:Ac** Anonymous. [Advertisement]. *IEEE Computer Architecture Letters*, 8(2):69, July/December 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano09e] **Anonymous:2009:Ad** Anonymous. [Advertisement]. *IEEE Computer Architecture Letters*, 8(2):70, July/December 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano09f] **Anonymous:2009:Ae** Anonymous. [Advertisement]. *IEEE Computer Architecture Letters*, 8(2):71, July/December 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano09g] **Anonymous:2009:Af** Anonymous. [Advertisement]. *IEEE Computer Architecture Letters*, 8(2):72, July/December 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano09h] **Anonymous:2009:EBCa** Anonymous. Editorial board [cover2]. *IEEE Computer Architecture Letters*, 8(1):c2, January/June 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano09i] **Anonymous:2009:EBCb** Anonymous. Editorial board [cover2]. *IEEE Computer Architecture Letters*, 8(2):c2, July/December 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano09j] **Anonymous:2009:FCa** Anonymous. [Front cover]. *IEEE Computer Architecture Letters*, 8(1):c1, January/June 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano09k] **Anonymous:2009:FCb** Anonymous. [Front cover]. *IEEE Computer Architecture Letters*, 8(2):c1, July/December 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano09l] **Anonymous:2009:ICSa** Anonymous. IEEE Computer Society [cover4]. *IEEE Computer Architecture Letters*, 8(1):c4, January/June 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [Ano09m] **Anonymous:2009:ICsb**
 Anonymous. IEEE Computer Society [cover4]. *IEEE Computer Architecture Letters*, 8(2):c4, July/December 2009. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano09n] **Anonymous:2009:IAa**
 Anonymous. Information for authors. *IEEE Computer Architecture Letters*, 8(1):c3, January/June 2009. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano09o] **Anonymous:2009:IAb**
 Anonymous. Information for authors. *IEEE Computer Architecture Letters*, 8(2):c3, July/December 2009. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10a] **Anonymous:2010:ICsb**
 Anonymous. 2011 IEEE Computer Society simulator design competition. *IEEE Computer Architecture Letters*, 9(2):66, July/December 2010. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10b] **Anonymous:2010:AIT**
 Anonymous. Advertisement — *IEEE Transactions on Computers* celebrates 60 years. *IEEE Computer Architecture Letters*, 9(2):65, July/December 2010. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10c] **Anonymous:2010:ACS**
 Anonymous. Advertisement — Computer Society Digital Library. *IEEE Computer Architecture Letters*, 9(2):72, July/December 2010. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10d] **Anonymous:2010:ADY**
 Anonymous. Advertisement — distinguish yourself with the CSDP. *IEEE Computer Architecture Letters*, 9(2):68, July/December 2010. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10e] **Anonymous:2010:ASS**
 Anonymous. Advertisement — special student offer. *IEEE Computer Architecture Letters*, 9(2):67, July/December 2010. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10f] **Anonymous:2010:ASC**
 Anonymous. Advertisement — stay connected to the IEEE Computer Society. *IEEE Computer Architecture Letters*, 9(2):71, July/December 2010. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).

- [Ano10g] **Anonymous:2010:CPS** Anonymous. Conference Proceedings Services (CPS) [advertisement]. *IEEE Computer Architecture Letters*, 9(2):69, July/December 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10h] **Anonymous:2010:EBCa** Anonymous. Editorial board [cover2]. *IEEE Computer Architecture Letters*, 9(1):c2, January/June 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10i] **Anonymous:2010:EBCb** Anonymous. Editorial board [cover2]. *IEEE Computer Architecture Letters*, 9(2):c2, July/December 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10j] **Anonymous:2010:FCa** Anonymous. [Front cover]. *IEEE Computer Architecture Letters*, 9(1):c1, January/June 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10k] **Anonymous:2010:FCb** Anonymous. [Front cover]. *IEEE Computer Architecture Letters*, 9(2):c1, July/December 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10l] **Anonymous:2010:ICSa** Anonymous. IEEE Computer Society [cover4]. *IEEE Computer Architecture Letters*, 9(1):c4, January/June 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10m] **Anonymous:2010:ICSd** Anonymous. IEEE Computer Society [cover4]. *IEEE Computer Architecture Letters*, 9(2):c4, July/December 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10n] **Anonymous:2010:ICSc** Anonymous. IEEE Computer Society jobs. *IEEE Computer Architecture Letters*, 9(2):70, July/December 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10o] **Anonymous:2010:IAa** Anonymous. Information for authors. *IEEE Computer Architecture Letters*, 9(1):c3, January/June 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano10p] **Anonymous:2010:IAb** Anonymous. Information for authors. *IEEE Computer Architecture Letters*, 9(2):c3, July/December 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [Ano11a] **Anonymous:2011:AI** Anonymous. 2010 annual index. *IEEE Computer Architecture Letters*, 10(1):??, January/June 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano11b] **Anonymous:2011:RL** Anonymous. 2010 reviewers list. *IEEE Computer Architecture Letters*, 10(1):28, January/June 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano11c] **Anonymous:2011:Ca** Anonymous. Cover 2. *IEEE Computer Architecture Letters*, 10(1):c2, January/June 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano11d] **Anonymous:2011:Cb** Anonymous. Cover 3. *IEEE Computer Architecture Letters*, 10(1):c3, January/June 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano11e] **Anonymous:2011:Cd** Anonymous. Cover 3. *IEEE Computer Architecture Letters*, 10(2):c3, July/December 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano11f] **Anonymous:2011:Cc** Anonymous. Cover 4. *IEEE Computer Architecture Letters*, 10(1):c4, January/June 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano11g] **Anonymous:2011:FCa** Anonymous. [Front cover]. *IEEE Computer Architecture Letters*, 10(1):c1, January/June 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano11h] **Anonymous:2011:FCb** Anonymous. [Front cover]. *IEEE Computer Architecture Letters*, 10(2):c1, July/December 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano11i] **Anonymous:2011:ICS** Anonymous. IEEE Computer Society [society information]. *IEEE Computer Architecture Letters*, 10(2):c4, July/December 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano11j] **Anonymous:2011:PI** Anonymous. Publication information. *IEEE Computer Architecture Letters*, 10(2):c2, July/December 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [Ano12a] **Anonymous:2012:AI** Anonymous. 2011 annual index. *IEEE Computer Architecture Letters*, 11(1):??, January/June 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano12b] **Anonymous:2012:RL** Anonymous. 2011 reviewers list. *IEEE Computer Architecture Letters*, 11(1):25–26, January/June 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano12c] **Anonymous:2012:ACP** Anonymous. Advertisement — Conference Publishing Services (CPS). *IEEE Computer Architecture Letters*, 11(1):28, January/June 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano12d] **Anonymous:2012:BC** Anonymous. [Back cover]. *IEEE Computer Architecture Letters*, 11(2):c4, July/December 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano12e] **Anonymous:2012:BIC** Anonymous. [Back inside cover]. *IEEE Computer Architecture Letters*, 11(2):c3, July/December 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano12f] **Anonymous:2012:Ca** Anonymous. [Cover2]. *IEEE Computer Architecture Letters*, 11(1):c2, January/June 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano12g] **Anonymous:2012:Cb** Anonymous. [Cover3]. *IEEE Computer Architecture Letters*, 11(1):c3, January/June 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano12h] **Anonymous:2012:FCT** Anonymous. [Front cover and table of contents]. *IEEE Computer Architecture Letters*, 11(1):c1, January/June 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano12i] **Anonymous:2012:FIC** Anonymous. [Front inside cover]. *IEEE Computer Architecture Letters*, 11(2):c2, July/December 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano12j] **Anonymous:2012:ICS** Anonymous. IEEE Computer Society [back cover]. *IEEE Computer Architecture Letters*, 11(1):c4, January/June 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [Ano12k] **Anonymous:2012:TNQ** Anonymous. There now is a quick and easy way to find out about our collection of *Transactions* [advertisement]. *IEEE Computer Architecture Letters*, 11(1):26, January/June 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano13a] **Anonymous:2013:AI** Anonymous. 2012 annual index. *IEEE Computer Architecture Letters*, 12(1):1–4, January/June 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano13b] **Anonymous:2013:RL** Anonymous. 2012 reviewers list. *IEEE Computer Architecture Letters*, 12(1):33–34, January/June 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano13c] **Anonymous:2013:BC** Anonymous. [Back cover]. *IEEE Computer Architecture Letters*, 12(2):c4, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano13d] **Anonymous:2013:BIC** Anonymous. [Back inside cover]. *IEEE Computer Architecture Letters*, 12(2):c3, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano13e] **Anonymous:2013:ITN** Anonymous. *IEEE Transactions* newsletter. *IEEE Computer Architecture Letters*, 12(1):36, January/June 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano13f] **Anonymous:2013:FC** Anonymous. [Front cover]. *IEEE Computer Architecture Letters*, 12(2):c1, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano13g] **Anonymous:2013:FIC** Anonymous. [Front inside cover]. *IEEE Computer Architecture Letters*, 12(2):c2, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano13h] **Anonymous:2013:IOAa** Anonymous. IEEE open access publishing. *IEEE Computer Architecture Letters*, 12(1):35, January/June 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano13i] **Anonymous:2013:IOAb** Anonymous. IEEE open access publishing. *IEEE Computer Architecture Letters*, 12(2):71, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [Ano13j] **Anonymous:2013:SCI** Anonymous. Stay connected to the IEEE Computer Society. *IEEE Computer Architecture Letters*, 12(2):72, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano14a] **Anonymous:2014:ICAa** Anonymous. *IEEE Computer Architecture Letters* Editorial Board. *IEEE Computer Architecture Letters*, 13(2):C2, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano14b] **Anonymous:2014:ICAb** Anonymous. *IEEE Computer Architecture Letters* information for authors. *IEEE Computer Architecture Letters*, 13(2):C3, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano14c] **Anonymous:2014:ITPa** Anonymous. *IEEE Transactions on Pattern Analysis and Machine Intelligence* Editorial Board. *IEEE Computer Architecture Letters*, 13(1):C2, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano14d] **Anonymous:2014:ITPb** Anonymous. *IEEE Transactions on Pattern Analysis and Machine Intelligence* information for authors. *IEEE Computer Architecture Letters*, 13(1):C3, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano14e] **Anonymous:2014:ICSa** Anonymous. IEEE Computer Society. *IEEE Computer Architecture Letters*, 13(1):C4, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano14f] **Anonymous:2014:ICSb** Anonymous. IEEE Computer Society [advertisement]. *IEEE Computer Architecture Letters*, 13(2):C4, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano14g] **Anonymous:2014:TCa** Anonymous. Table of contents. *IEEE Computer Architecture Letters*, 13(1):C1–C4, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano14h] **Anonymous:2014:TCb** Anonymous. Table of contents. *IEEE Computer Architecture Letters*, 13(2):C1, July/December 2014. CODEN ???? ISSN 1556-

6056 (print), 1556-6064 (electronic).

Anonymous:2015:IIC

- [Ano15a] Anonymous. 2014 index *IEEE Computer Architecture Letters* vol. 13. *IEEE Computer Architecture Letters*, 14(1):1–5, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Anonymous:2015:ICAa

- [Ano15b] Anonymous. *IEEE Computer Architecture Letters* Editorial Board. *IEEE Computer Architecture Letters*, 14(1):C2, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Anonymous:2015:ICAc

- [Ano15c] Anonymous. *IEEE Computer Architecture Letters* Editorial Board. *IEEE Computer Architecture Letters*, 14(2):C2, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Anonymous:2015:ICAb

- [Ano15d] Anonymous. *IEEE Computer Architecture Letters* information for authors. *IEEE Computer Architecture Letters*, 14(1):C3, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

[Ano15e]

Anonymous:2015:ICAd

Anonymous. *IEEE Computer Architecture Letters* information for authors. *IEEE Computer Architecture Letters*, 14(2):C3, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Anonymous:2015:ICSa

[Ano15f]

Anonymous. IEEE Computer Society. *IEEE Computer Architecture Letters*, 14(1):C4, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Anonymous:2015:ICSb

[Ano15g]

Anonymous. IEEE Computer Society. *IEEE Computer Architecture Letters*, 14(2):C4, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Anonymous:2015:RSC

[Ano15h]

Anonymous. Rock stars of cybersecurity 2015 conference. *IEEE Computer Architecture Letters*, 14(1):84, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Anonymous:2015:RSW

[Ano15i]

Anonymous. Rock stars of wearables. *IEEE Computer Architecture Letters*, 14(1):83, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [Ano15j] **Anonymous:2015:TCa**
Anonymous. Table of contents. *IEEE Computer Architecture Letters*, 14(1):C1, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano15k] **Anonymous:2015:TCb**
Anonymous. Table of contents. *IEEE Computer Architecture Letters*, 14(2):C1, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano16a] **Anonymous:2016:IICa**
Anonymous. 2015 index *IEEE Computer Architecture Letters* vol. 14. *IEEE Computer Architecture Letters*, 15(1):1–6, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano16b] **Anonymous:2016:IICb**
Anonymous. 2015 index *IEEE Computer Architecture Letters* vol. 14. *IEEE Computer Architecture Letters*, 15(1):1–6, January/June 2016. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano16c] **Anonymous:2016:BC**
Anonymous. [Back cover]. *IEEE Computer Architecture Letters*, 15(1):C4, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano16d] **Anonymous:2016:ICS**
Anonymous. *IEEE Cyber Security. IEEE Computer Architecture Letters*, 15(1):68, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano16e] **Anonymous:2016:Ca**
Anonymous. Cover. *IEEE Computer Architecture Letters*, 15(1):C2, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano16f] **Anonymous:2016:Cb**
Anonymous. Cover. *IEEE Computer Architecture Letters*, 15(1):C2, January/June 2016. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano16g] **Anonymous:2016:Cc**
Anonymous. Cover. *IEEE Computer Architecture Letters*, 15(1):C3, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano16h] **Anonymous:2016:Cd**
Anonymous. Cover. *IEEE Computer Architecture Letters*, 15(1):C3, January/June 2016. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano16i] **Anonymous:2016:Ce**
Anonymous. Cover. *IEEE Computer Architecture Letters*, 15(2):C2, July/December

2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Anonymous:2016:Cf

[Ano16j] Anonymous. Cover. *IEEE Computer Architecture Letters*, 15(2):C3, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Ano16o]

Anonymous:2016:ENM

[Ano16k] Anonymous. Experience the newest and most advanced thinking in big data analytics. *IEEE Computer Architecture Letters*, 15(1):67, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Ano16p]

Anonymous:2016:IICc

[Ano16l] Anonymous. Introducing IEEE Collabratec. *IEEE Computer Architecture Letters*, 15(1):66, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Ano17]

Anonymous:2016:IICd

[Ano16m] Anonymous. Introducing IEEE Collabratec. *IEEE Computer Architecture Letters*, 15(1):66, January/June 2016. ISSN 1556-6056 (print), 1556-6064 (electronic). [Ano18]

Anonymous:2016:TCa

[Ano16n] Anonymous. Table of contents. *IEEE Computer Architecture Letters*, 15(1):C1,

January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Anonymous:2016:TCb

Anonymous. Table of contents. *IEEE Computer Architecture Letters*, 15(2):C1, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Anonymous:2016:TCBa

Anonymous. Table of contents [back cover]. *IEEE Computer Architecture Letters*, 15(2):C4, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Anonymous:2017:IIC

Anonymous. 2016 index *IEEE Computer Architecture Letters* vol. 15. *IEEE Computer Architecture Letters*, 16(1):1–6, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Anonymous:2018:IIC

Anonymous. 2017 index *IEEE Computer Architecture Letters* vol. 16. *IEEE Computer Architecture Letters*, 17(1):1–6, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [Ano19] **Anonymous:2019:IIC**
 Anonymous. 2018 index *IEEE Computer Architecture Letters* vol. 17. *IEEE Computer Architecture Letters*, 18(1):1–8, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano20] **Anonymous:2020:IIC**
 Anonymous. 2019 index *IEEE Computer Architecture Letters* vol. 18. *IEEE Computer Architecture Letters*, 19(1):1–8, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano21] **Anonymous:2021:IIC**
 Anonymous. 2020 index *IEEE Computer Architecture Letters* vol. 19. *IEEE Computer Architecture Letters*, 20(1):1–7, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ano22] **Anonymous:2022:IIC**
 Anonymous. 2021 index *IEEE Computer Architecture Letters* vol. 20. *IEEE Computer Architecture Letters*, 21(1):1–8, January/June 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ant09] **Antelo:2009:CBF**
 Elisardo Antelo. A comment on “Beyond Fat-tree: Unidirectional Load-Balanced Multistage Interconnection Network””. *IEEE Computer Architecture Letters*, 8(1):33–34, January/June 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). See [GVG⁺08].
- [APK⁺18] **Ajdari:2018:SHB**
 Mohammadamin Ajdari, Pyeongsu Park, Dongup Kwon, Joon-sung Kim, and Jangwoo Kim. A scalable HW-based inline deduplication for SSD arrays. *IEEE Computer Architecture Letters*, 17(1):47–50, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [APK⁺21] **Amarnath:2021:HAS**
 Aporva Amarnath, Subhankar Pal, Hiwot Tadese Kassa, Augusto Vega, Alper Buyuktosunoglu, Hubertus Franke, John-David Wellman, Ronald Dreslinski, and Pradip Bose. Heterogeneity-aware scheduling on SoCs for autonomous vehicles. *IEEE Computer Architecture Letters*, 20(2):82–85, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [AQ24] **Ayanzadeh:2024:ERR**
 Ramin Ayanzadeh and Moinuddin Qureshi. Enhancing the reach and reliability of quantum annealers by pruning longer chains. *IEEE Computer Architecture Letters*, 23(1):25–28, January/

June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).

Arelakis:2014:CVA

[AS14]

Angelos Arelakis and Per Stenström. A case for a value-aware cache. *IEEE Computer Architecture Letters*, 13(1):1–4, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Almatrood:2018:DGP

[AS18]

Amjad F. Almatrood and Harpreet Singh. Design of generalized pipeline cellular array in quantum-dot cellular automata. *IEEE Computer Architecture Letters*, 17(1):29–32, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Alian:2021:IOI

[ASK⁺21]

Mohammad Alian, Jongmin Shin, Ki-Dong Kang, Ren Wang, Alexandros Daglis, Daehoon Kim, and Nam Sung Kim. IDIO: Orchestrating inbound network data on server processors. *IEEE Computer Architecture Letters*, 20(1):30–33, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).

Aimoniotis:2021:RBC

[ASSK21]

Pavlos Aimoniotis, Christos Sakalis, Magnus Sjölander,

and Stefanos Kaxiras. Re-order buffer contention: a forward speculative interference attack for speculation invariant instructions. *IEEE Computer Architecture Letters*, 20(2):162–165, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).

Altaf:2015:LPM

[AW15]

Muhammad Shoaib Bin Altaf and David A. Wood. LogCA: a performance model for hardware accelerators. *IEEE Computer Architecture Letters*, 14(2):132–135, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Angstadt:2018:MOS

[AWD⁺18]

Kevin Angstadt, Jack Wadden, Vinh Dang, Ted Xie, Dan Kramp, Westley Weimer, Mircea Stan, and Kevin Skadron. MNCaRT: an open-source, multi-architecture automata-processing research and execution ecosystem. *IEEE Computer Architecture Letters*, 17(1):84–87, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Accetti:2022:SCE

[AYL22]

Cecil Accetti, Rendong Ying, and Peilin Liu. Structured combinators for efficient graph reduction. *IEEE Computer Architecture Letters*, 21(2):73–76, July/December

2022. ISSN 1556-6056 (print), 1556-6064 (electronic).

Barber:2019:ISD

[BBZ⁺19]

Kristin Barber, Anys Bacha, Li Zhou, Yinqian Zhang, and Radu Teodorescu. Isolating speculative data to prevent transient execution attacks. *IEEE Computer Architecture Letters*, 18(2):178–181, July 2019. ISSN 1556-6064.

Balfour:2008:EEP

[BDBS⁺08]

J. Balfour, W. Dally, D. Black-Schaffer, V. Parikh, and J. Park. An energy-efficient processor architecture for embedded systems. *IEEE Computer Architecture Letters*, 7(1):29–32, January 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Bracy:2006:DAC

[BDJ06]

A. Bracy, K. Doshi, and Q. Jacobson. Disintermediated active communication. *IEEE Computer Architecture Letters*, 5(2):15, February 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Blem:2013:MMA

[BEA⁺13]

Emily Blem, Hadi Esmaeilzadeh, Renee St Amant, Karthikeyan Sankaralingam, and Doug Burger. Multicore model from abstract single core inputs. *IEEE Computer Architecture Letters*, 12(2):

59–62, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Bae:2023:ISF

[BGL⁺23]

Hanyeoreum Bae, Donghyun Gouk, Seungjun Lee, Jiseon Kim, Sungjoon Koh, Jie Zhang, and Myoungsoo Jung. Intelligent SSD firmware for zero-overhead journaling. *IEEE Computer Architecture Letters*, 22(1):25–28, January/June 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).

Boroumand:2017:LEC

[BGP⁺17]

Amirali Boroumand, Saugata Ghose, Minesh Patel, Hasan Hassan, Brandon Lucia, Kevin Hsieh, Krishna T. Malladi, Hongzhong Zheng, and Onur Mutlu. LazyPIM: an efficient cache coherence mechanism for processing-in-memory. *IEEE Computer Architecture Letters*, 16(1):46–50, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Bodduna:2020:BRs

[BGS⁺20]

Rahul Bodduna, Vinod Ganesan, Patanjali SLPSK, Kamakoti Veezhinathan, and Chester Rebeiro. Brutus: Refuting the security claims of the cache timing randomization countermeasure proposed in CEASER. *IEEE Computer*

- Architecture Letters*, 19(1):9–12, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic). [BHY⁺19]
- [BGZT22] Kristin Barber, Moein Ghaniyoun, Yinqian Zhang, and Radu Teodorescu. A pre-silicon approach to discovering microarchitectural vulnerabilities in security critical applications. *IEEE Computer Architecture Letters*, 21(1):9–12, January/June 2022. ISSN 1556-6056 (print), 1556-6064 (electronic). [BKA⁺09]
- [BHD09] James Balfour, R. Curtis Harting, and William J. Dally. Operand registers and explicit operand forwarding. *IEEE Computer Architecture Letters*, 8(2):60–63, July/December 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [BLKSA17]
- [BHL⁺18] Abanti Basak, Xing Hu, Shuangchen Li, Sang Min Oh, and Yuan Xie. Exploring core and cache hierarchy bottlenecks in graph processing workloads. *IEEE Computer Architecture Letters*, 17(2):197–200, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [BLM06]
- [Bhardwaj:2019:DOC] K. Bhardwaj, M. Havasi, Y. Yao, D. M. Brooks, J. M. H. Lobato, and G. Wei. Determining optimal coherency interface for many-accelerator SoCs using Bayesian optimization. *IEEE Computer Architecture Letters*, 18(2):119–123, July 2019. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Baldassin:2009:CEC] Alexandro Baldassin, Felipe Klein, Guido Araujo, Rodolfo Azevedo, and Paulo Centoducatte. Characterizing the energy consumption of software transactional memory. *IEEE Computer Architecture Letters*, 8(2):56–59, July/December 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Bakhshalipour:2017:ETD] Mohammad Bakhshalipour, Pejman Lotfi-Kamran, and Hamid Sarbazi-Azad. An efficient temporal data prefetcher for L1 caches. *IEEE Computer Architecture Letters*, 16(2):99–102, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Blundell:2006:STM] C. Blundell, E. C. Lewis, and M. M. K. Martin.

- Subtleties of transactional memory atomicity semantics. *IEEE Computer Architecture Letters*, 5(2):17, February 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [BSBD⁺08]
- [BREM08] A. Biswas, P. Racunas, J. Emer, and S. Mukherjee. Computing accurate AVFs using ACE analysis on performance models: a rebuttal. *IEEE Computer Architecture Letters*, 7(1):21–24, January 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [BSD⁺19]
- [BRUS21] Nirmal Kumar Boran, Shubhankit Rathore, Meet Udeshi, and Virendra Singh. Fine-grained scheduling in heterogeneous-ISA architectures. *IEEE Computer Architecture Letters*, 20(1):9–12, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic). [BSMB23]
- [BS17] Nathan Beckmann and Daniel Sanchez. Cache calculus: Modeling caches through differential equations. *IEEE Computer Architecture Letters*, 16(1):1–5, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [BVL09]
- [Black-Schaffer:2008:HIR] D. Black-Schaffer, J. Balfour, W. Dally, V. Parikh, and J. Park. Hierarchical instruction register organization. *IEEE Computer Architecture Letters*, 7(2):41–44, July 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Balaji:2019:FEW] Adarsha Balaji, Shihao Song, Anup Das, Nikil Dutt, Jeff Krichmar, Nagarajan Kandasamy, and Francky Catthoor. A framework to explore workload-specific performance and lifetime trade-offs in neuromorphic computing. *IEEE Computer Architecture Letters*, 18(2):149–152, July 2019. ISSN 1556-6064.
- [Braná:2023:KSC] Jennifer Braná, Brian C. Schwedock, Yatin A. Manerkar, and Nathan Beckmann. Kobold: Simplified cache coherence for cache-attached accelerators. *IEEE Computer Architecture Letters*, 22(1):41–44, January/June 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Barnes:2009:XBA] Christopher Barnes, Pranav Vaidya, and Jaehwan John Lee. An XML-based ADL framework for automatic generation of multithreaded com-

- puter architecture simulators. *IEEE Computer Architecture Letters*, 8(1):13–16, January/June 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [CE14]
- [BY17] Abdel-Hameed A. Badawy and Donald Yeung. Guiding locality optimizations for graph computations via reuse distance analysis. *IEEE Computer Architecture Letters*, 16(2):119–122, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). **Badawy:2017:GLO**
- [CAPS09] Derek Chiou, Hari Angepat, Nikhil A. Patil, and Dam Sunwoo. Accurate functional-first multicore simulators. *IEEE Computer Architecture Letters*, 8(2):64–67, July/December 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). **Chiou:2009:AFF**
- [CCWY17] Li-Jhan Chen, Hsiang-Yun Cheng, Po-Han Wang, and Chia-Lin Yang. Improving GPGPU performance via cache locality aware thread block scheduling. *IEEE Computer Architecture Letters*, 16(2):127–131, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). **Chen:2017:IGP**
- [CFM⁺03] A. Cohen, F. Finkelstein, A. Mendelson, R. Ronen, and D. Rudoy. On estimating optimal performance of CPU dynamic thermal management. *IEEE Computer Architecture Letters*, 2(1):6, January 2003. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). **Cohen:2003:EOP**
- [CEA18] Esha Choukse, Mattan Erez, and Alaa Alameldeen. CompressPoints: an evaluation methodology for compressed memory systems. *IEEE Computer Architecture Letters*, 17(2):126–129, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). **Choukse:2018:CEM**
- [CF24] Caden Corontzos and Eitan Frachtenberg. Direct-coding DNA with multilevel parallelism. *IEEE Computer Architecture Letters*, 23(1):21–24, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic). **Corontzos:2024:DCD**
- [CFM⁺03] Yaman Çakmakçi and Oğuz Ergin. Exploiting virtual addressing for increasing reliability. *IEEE Computer Architecture Letters*, 13(1):29–32, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). **Çakmakçi:2014:EVA**

- [CGY⁺14] **Chen:2014:PEC** Zheng Chen, Huaxi Gu, Yintang Yang, Luying Bai, and Hui Li. A power efficient and compact optical interconnect for network-on-chip. *IEEE Computer Architecture Letters*, 13(1):5–8, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CHK⁺18] **Chowdhury:2018:EMP** Zamshed Chowdhury, Jonathan D. Harms, S. Karen Khatamifard, Masoud Zabihi, Yang Lv, Andrew P. Lyle, Sachin S. Sapatnekar, Ulya R. Karpuzcu, and Jian-Ping Wang. Efficient in-memory processing using spintronics. *IEEE Computer Architecture Letters*, 17(1):42–46, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Cit04] **Citron:2004:ELE** D. Citron. Exploiting low entropy to reduce wire delay. *IEEE Computer Architecture Letters*, 3(1):1, January 2004. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CKA20] **Choe:2020:SMP** Wonkyo Choe, Jonghyeon Kim, and Jeongseob Ahn. A study of memory placement on hardware-assisted tiered memory systems. *IEEE Computer Architecture Letters*, 19(2):122–125, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CKZ⁺20] **Chowdhury:2020:VNM** Zamshed I. Chowdhury, S. Karen Khatamifard, Zhaoyong Zheng, Tali Moreshet, R. Iris Bahar, and Ulya R. Karpuzcu. Voltage noise mitigation with barrier approximation. *IEEE Computer Architecture Letters*, 19(2):155–158, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CLCG14] **Chou:2014:EPE** Yu-Liang Chou, Shaoshan Liu, Eui-Young Chung, and Jean-Luc Gaudiot. An energy and performance efficient DVFS scheme for irregular parallel divide-and-conquer algorithms on the Intel SCC. *IEEE Computer Architecture Letters*, 13(1):13–16, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CLJ⁺02] **Choi:2002:LPT** Jin-Hyuck Choi, Jung-Hoon Lee, Seh-Woong Jeong, Shin-Dug Kim, and C. Weems. A low power TLB structure for embedded systems. *IEEE Computer Architecture Letters*, 1(1):3, January 2002. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [CM08] **Cho:2008:CAL** S. Cho and R. Melhem. Corollaries to Amdahl’s Law for energy. *IEEE Computer Architecture Letters*, 7(1):25–28, January 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CMLV03] **Cristal:2003:CRC** A. Cristal, J. F. Martinez, J. Llosa, and M. Valero. A case for resource-conscious out-of-order processors. *IEEE Computer Architecture Letters*, 2(1):7, January 2003. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CMP+14] **Cota:2014:AMR** [CSSU20] Emilio G. Cota, Paolo Mantovani, Michele Petracca, Mario R. Casu, and Luca P. Carloni. Accelerator memory reuse in the dark silicon era. *IEEE Computer Architecture Letters*, 13(1):9–12, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CNHH15] **Carlson:2015:EPM** [CST+04] Trevor E. Carlson, Siddharth Nilakantan, Mark Hempstead, and Wim Heirman. Epoch profiles: Microarchitecture-based application analysis and optimization. *IEEE Computer Architecture Letters*, 14(1):30–33, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CPK+23] **Choi:2023:UPP** Jaewan Choi, Jaehyun Park, Kwanhee Kyung, Nam Sung Kim, and Jung Ho Ahn. Unleashing the potential of PIM: Accelerating large batched inference of transformer-based generative models. *IEEE Computer Architecture Letters*, 22(2):113–116, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Cavus:2020:EPP** Mustafa Cavus, Mohammed Shatnawi, Resit Sendag, and Augustus K. Uht. Exploring prefetching, pre-execution and branch outcome streaming for in-memory database lookups. *IEEE Computer Architecture Letters*, 19(1):5–8, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Ceze:2004:CHL** L. Ceze, K. Strauss, J. Tuck, J. Renau, and J. Torrellas. CAVA: Hiding L2 misses with checkpoint-assisted value prediction. *IEEE Computer Architecture Letters*, 3(1):7, January 2004. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [CTJ+17] **Carlson:2017:THL**
Trevor E. Carlson, Kim-Anh Tran, Alexandra Jimborean, Konstantinos Koukos, Magnus Sjölander, and Stefanos Kaxiras. Transcending hardware limits with software out-of-order processing. *IEEE Computer Architecture Letters*, 16(2):162–165, July/December 2017. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CTL+20] **Chu:2020:HPD**
Zhufei Chu, Huiming Tian, Zeqiang Li, Yinshui Xia, and Lunyao Wang. A high-performance design of generalized pipeline cellular array. *IEEE Computer Architecture Letters*, 19(1):47–50, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CTNL16] **Cakmakci:2016:CPG**
Yaman Çakmakçi, Will Toms, Javier Navaridas, and Mikel Lujan. Cyclic power-gating as an alternative to voltage and frequency scaling. *IEEE Computer Architecture Letters*, 15(2):77–80, July/December 2016. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CV15] **Chen:2015:HSC**
Jie Chen and Guru Venkataramani. A hardware-software cooperative approach for application energy profiling. *IEEE Computer Architecture Letters*, 14(1):5–8, January/June 2015. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CVF+24] **Cho:2024:EEA**
Minsik Cho, Keivan A. Vahid, Qichen Fu, Saurabh Adya, Carlo C. Del Mundo, Mohammad Rastegari, Devang Naik, and Peter Zatloukal. eDKM: an efficient and accurate train-time weight clustering for large language models. *IEEE Computer Architecture Letters*, 23(1):37–40, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CVP12] **Chen:2012:NPD**
Jie Chen, Guru Venkataramani, and Gabriel Parmer. The need for power debugging in the multi-core environment. *IEEE Computer Architecture Letters*, 11(2):57–60, July/December 2012. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CWK+22] **Chacon:2022:HTT**
Gino A. Chacon, Charles Williams, Johann Knechtel, Ozgur Sinanoglu, and Paul V. Gratz. Hardware Trojan threats to cache coherence in modern 2.5D chiplet systems. *IEEE Computer Architecture Letters*, 21(2):133–136, July/December 2022. ISSN 1556-

- 6056 (print), 1556-6064 (electronic).
- [CXS18] Eleftherios-Iordanis Christoforidis, Sotirios Xydis, and Dimitrios Soudris. CF-TUNE: Collaborative filtering auto-tuning for energy efficient many-core processors. *IEEE Computer Architecture Letters*, 17(1):25–28, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CYAW20] Yuezhi Che, Yuanzhou Yang, Amro Awad, and Rujia Wang. A lightweight memory access pattern obfuscation framework for NVM. *IEEE Computer Architecture Letters*, 19(2):163–166, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [CZYY11] Inseok Choi, Minshu Zhao, Xu Yang, and Donald Yeung. Experience with improving distributed shared cache performance on Tiler’s Tile processor. *IEEE Computer Architecture Letters*, 10(2):45–48, July/December 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [DC18] Srdjan Durkovic and Zoran Cica. Birkhoff–von Neumann switch based on greedy scheduling. *IEEE Computer Architecture Letters*, 17(1):13–16, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [DCG12] Abhishek Deb, Josep Maria Codina, and Antonio Gonzalez. A HW/SW co-designed programmable functional unit. *IEEE Computer Architecture Letters*, 11(1):9–12, January/June 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [DD18] Sang Wook Stephen Do and Michel Dubois. Core reliability: Leveraging hardware transactional memory. *IEEE Computer Architecture Letters*, 17(2):105–108, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [DEC⁺18] Leila Delshadtehrani, Schuyler Eldridge, Sadullah Canakci, Manuel Egele, and Ajay Joshi. Nile: a programmable monitoring coprocessor. *IEEE Computer Architecture Letters*, 17(1):92–

- 95, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [DK13] **Delimitrou:2013:NCD** [DL20] Christina Delimitrou and Christos Kozyrakis. The Netflix challenge: Datacenter edition. *IEEE Computer Architecture Letters*, 12(1):29–32, January/June 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [DK16] **Delimitrou:2016:SID** [DM06] Christina Delimitrou and Christos Kozyrakis. Security implications of data mining in cloud scheduling. *IEEE Computer Architecture Letters*, 15(2):109–112, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [DKD07] **Dieter:2007:LCM** [DOM⁺07] W. R. Dieter, A. Kaveti, and H. G. Dietz. Low-cost microarchitectural support for improved floating-point accuracy. *IEEE Computer Architecture Letters*, 6(1):13–16, January 2007. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [DL19] **Denby:2019:OEC** [DOM⁺08] Bradley Denby and Brandon Lucia. Orbital edge computing: Machine inference in space. *IEEE Computer Architecture Letters*, 18(1):59–62, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Desai:2020:PAH** Harsh Desai and Brandon Lucia. A power-aware heterogeneous architecture scaling model for energy-harvesting computers. *IEEE Computer Architecture Letters*, 19(1):68–71, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Donald:2006:EPP** J. Donald and M. Martonosi. An efficient, practical parallelization methodology for multicore architecture simulation. *IEEE Computer Architecture Letters*, 5(2):14, February 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Das:2007:MMC** A. Das, S. Ozdemir, G. Memik, J. Zambreno, and A. Choudhary. Microarchitectures for managing chip revenues under process variations. *IEEE Computer Architecture Letters*, 6(2):29–32, February 2007. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Das:2008:MMC** A. Das, S. Ozdemir, G. Memik, J. Zambreno, and A. Choudhary. Microarchitectures for

- managing chip revenues under process variations. *IEEE Computer Architecture Letters*, 7(1):5–8, January 2008. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic). [DS09]
- [DPC16] Bhavya K. Daya, Li-Shiuan Peh, and Anantha P. Chandrakasan. Towards high-performance bufferless NoCs with SCEPTER. *IEEE Computer Architecture Letters*, 15(1):62–65, January/June 2016. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [DPP23] Chandana S. Deshpande, Arthur Perais, and Frédéric Pétrot. Toward practical 128-bit general purpose microarchitectures. *IEEE Computer Architecture Letters*, 22(2):81–84, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [DRGA12] John D. Davis, Suzanne Rivoire, Moises Goldszmidt, and Ehsan K. Ardestani. Including variability in large-scale cluster power models. *IEEE Computer Architecture Letters*, 11(2):29–32, July/December 2012. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic). [DVAE18]
- [Desai:2009:AIC] Aniruddha Desai and Jugdutt Singh. Architecture independent characterization of embedded Java workloads. *IEEE Computer Architecture Letters*, 8(1):29–32, January/June 2009. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Delimitrou:2012:DDS] Christina Delimitrou, Sriram Sankar, Kushagra Vaid, and Christos Kozyrakis. Decoupling datacenter storage studies from access to large-scale applications. *IEEE Computer Architecture Letters*, 11(2):53–56, July/December 2012. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic). [DSVK12]
- [Dung:2013:CAS] Nam Duong and Alexander V. Veidenbaum. Compiler-assisted, selective out-of-order commit. *IEEE Computer Architecture Letters*, 12(1):21–24, January/June 2013. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Davis:2012:IVL] John D. Davis, Suzanne Rivoire, Moises Goldszmidt, and Ehsan K. Ardestani. Including variability in large-scale cluster power models. *IEEE Computer Architecture Letters*, 11(2):29–32, July/December 2012. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic). [DVAE18]
- [DePestel:2018:RRP] Sander De Pestel, Sam Van den Steen, Shoaib Akram, and Lieven Eeckhout. RPPM: Rapid performance prediction of multithreaded applications on multicore hardware.

IEEE Computer Architecture Letters, 17(2):183–186, July/December 2018. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic). [Eec13]

Diamantopoulos:2015:MMI

[DXSS15] Dionysios Diamantopoulos, Sotirios Xydis, Kostas Siozios, and Dimitrios Soudris. Mitigating memory-induced dark silicon in many-accelerator architectures. *IEEE Computer Architecture Letters*, 14(2):136–139, July/December 2015. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic). [Eec22]

Eyerman:2014:RCW

[EE14] Stijn Eyerman and Lieven Eeckhout. Restating the case for weighted-IPC metrics to evaluate multiprogram workload performance. *IEEE Computer Architecture Letters*, 13(2):93–96, July/December 2014. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic). [Eec24]

Eker:2016:EEC

[EE16] Abdulaziz Eker and Oğuz Ergin. Exploiting existing copies in register file for soft error correction. *IEEE Computer Architecture Letters*, 15(1):17–20, January/June 2016. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic). [EF07]

Eeckhout:2013:MNE

Lieven Eeckhout. A message from the new Editor-in-Chief and introduction of new Associate Editors. *IEEE Computer Architecture Letters*, 12(1):2, January/June 2013. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).

Eeckhout:2022:FOM

Lieven Eeckhout. A first-order model to assess computer architecture sustainability. *IEEE Computer Architecture Letters*, 21(2):137–140, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).

Eeckhout:2024:RPG

Lieven Eeckhout. R.I.P. geometric speedup use equal-work (or equal-time) harmonic mean speedup instead. *IEEE Computer Architecture Letters*, 23(1):78–82, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).

Etsion:2007:PPT

Y. Etsion and D. G. Feitelson. Probabilistic prediction of temporal locality. *IEEE Computer Architecture Letters*, 6(1):17–20, January 2007. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).

- [EGWM14] **Efracim:2014:EAR**
 Rotem Efracim, Ran Ginosar, C. Weiser, and Avi Mendelson. Energy aware race to halt: a down to EARtH approach for platform energy management. *IEEE Computer Architecture Letters*, 13(1):25–28, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [EHDH18] **Eyerman:2018:MSC**
 Stijn Eyerman, Wim Heirman, Kristof Du Bois, and Ibrahim Hur. Multi-stage CPI stacks. *IEEE Computer Architecture Letters*, 17(1):55–58, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [EHDH20] **Eyerman:2020:BOB**
 Stijn Eyerman, Wim Heirman, Sam Van den Steen, and Ibrahim Hur. Breaking in-order branch miss recovery. *IEEE Computer Architecture Letters*, 19(1):30–33, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [EHH21] **Eyerman:2021:MDT**
 Stijn Eyerman, Wim Heirman, and Ibrahim Hur. Modeling DRAM timing in parallel simulators with immediate-response memory model. *IEEE Computer Architecture Letters*, 20(2):90–93, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [EOA+23] **Escofet:2023:HQA**
 Pau Escofet, Anabel Ovide, Carmen G. Almudever, Eduard Alarcón, and Sergi Abadal. Hungarian qubit assignment for optimized mapping of quantum circuits on multi-core architectures. *IEEE Computer Architecture Letters*, 22(2):161–164, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [EPS06] **Eisley:2006:NCC**
 N. Eisley, Li-Shiuan Peh, and Li Shang. In-network cache coherence. *IEEE Computer Architecture Letters*, 5(1):34–37, January 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [EUVG06] **Ergin:2006:ENV**
 O. Ergin, O. Unsal, X. Vera, and A. Gonzalez. Exploiting narrow values for soft error tolerance. *IEEE Computer Architecture Letters*, 5(2):12, February 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [FAR+23] **Feng:2023:SOW**
 Justin Feng, Fatemeh Arkannezhad, Christopher Ryu, Enoch Huang, Siddhant

- Gupta, and Nader Sehatbakhsh. Simulating our way to safer software: a tale of integrating microarchitecture simulation and leakage estimation modeling. *IEEE Computer Architecture Letters*, 22(2):109–112, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic). [FHL+10]
- France:2024:RSA**
- [FBN+24] Loïc France, Florent Bruguier, David Novo, Maria Mushtaq, and Pascal Benoit. Reducing the silicon area overhead of counter-based rowhammer mitigations. *IEEE Computer Architecture Letters*, 23(1):61–64, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic). [FJ08]
- Flich:2008:LBD**
- [FD08] J. Flich and J. Duato. Logic-based distributed routing for NoCs. *IEEE Computer Architecture Letters*, 7(1):13–16, January 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [FLSZ17]
- Farmahini-Farahani:2015:DAA**
- [FFAMK15] Amin Farmahini-Farahani, Jung Ho Ahn, Katherine Morrow, and Nam Sung Kim. DRAMA: an architecture for accelerated processing near memory. *IEEE Computer Architecture Letters*, 14(1):26–29, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [FPA+21]
- Fang:2010:BRP**
- Zhen Fang, Erik G. Hallnor, Bin Li, Michael Leddige, Donglai Dai, Seung Eun Lee, Srihari Makineni, and Ravi Iyer. Boomerang: Reducing power consumption of response packets in NoCs with minimal performance impact. *IEEE Computer Architecture Letters*, 9(2):49–52, July/December 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Fide:2008:PUS**
- S. Fide and S. Jenks. Proactive use of shared L3 caches to enhance cache communications in multi-core processors. *IEEE Computer Architecture Letters*, 7(2):57–60, July 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Feng:2017:HHC**
- Liang Feng, Hao Liang, Sharad Sinha, and Wei Zhang. HeteroSim: a heterogeneous CPU–FPGA simulator. *IEEE Computer Architecture Letters*, 16(1):38–41, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Falahati:2021:DAC**
- Hajar Falahati, Masoud Peyro, Hossein Amini, Mehran

- Taghian, Mohammad Sadrosa-**[Gau09]**
 dati, Pejman Lotfi-Kamran,
 and Hamid Sarbazi-Azad. Data-aware compression of
 neural networks. *IEEE Computer Architecture Letters*,
 20(2):94–97, July/December 2021. ISSN 1556-6056 (print),
 1556-6064 (electronic).
- Fariborz:2022:MSB**
 [FSO+22] Marjan Fariborz, Mahyar
 Samani, Terry O’Neill, Ja-
 son Lowe-Power, S. J. Ben
 Yoo, and Venkatesh Akella.
 A model for scalable and bal-
 anced accelerators for graph
 processing. *IEEE Computer Architecture Letters*, 21
 (2):149–152, July/December
 2022. ISSN 1556-6056 (print),
 1556-6064 (electronic).
- Finlayson:2012:OSP**
 [FUWT12] Ian Finlayson, Gang-Ryung
 Uh, David Whalley, and Gary
 Tyson. An overview of static
 pipelining. *IEEE Computer Architecture Letters*, 11(1):
 17–20, January/June 2012.
 CODEN ????. ISSN 1556-
 6056 (print), 1556-6064 (elec-
 tronic).
- Goudarzi:2023:SBP**
 [GAH+23] Maziar Goudarzi, Reza Az-
 imi, Julian Humecki, Faizaan
 Rehman, Richard Zhang,
 Chirag Sethi, Tanishq Bom-
 man, and Yuqi Yang. By-
 software branch prediction in
 loops. *IEEE Computer Architecture Letters*, 22(2):129–
 132, July/December 2023.
 ISSN 1556-6056 (print), 1556-
 6064 (electronic).
- Gaudiot:2009:INE**
 Jean-Luc Gaudiot. Introduc-
 ing the new Editor-in-Chief
 of *IEEE Computer Architec-
 ture Letters*. *IEEE Computer
 Architecture Letters*, 8(2):37–
 38, July/December 2009. CO-
 DEN ????. ISSN 1556-
 6056 (print), 1556-6064 (elec-
 tronic).
- Guz:2009:MCV**
 [GBK+09] Zvika Guz, Evgeny Bolotin,
 Idit Keidar, Avinoam Kolodny,
 Avi Mendelson, and Uri C.
 Weiser. Many-core vs. many-
 thread machines: Stay away
 from the valley. *IEEE
 Computer Architecture Let-
 ters*, 8(1):25–28, January/
 June 2009. CODEN ????.
 ISSN 1556-6056 (print), 1556-
 6064 (electronic).
- Golshan:2020:HPC**
 [GBS+20] Fatemeh Golshan, Moham-
 mad Bakhshalipour, Mehran
 Shakerinava, Ali Ansari, Pe-
 jman Lotfi-Kamran, and
 Hamid Sarbazi-Azad. Har-
 nassing pairwise-correlating
 data prefetching with runa-
 head metadata. *IEEE Com-
 puter Architecture Letters*, 19
 (2):130–133, July/December
 2020. ISSN 1556-6056 (print),
 1556-6064 (electronic).

- [GD06] **Gupta:2006:TOI**
A. K. Gupta and W. J. Dally. Topology optimization of interconnection networks. *IEEE Computer Architecture Letters*, 5(1):10–13, January 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [GD18] **Gan:2018:AIC**
Yu Gan and Christina Delimitrou. The architectural implications of cloud microservices. *IEEE Computer Architecture Letters*, 17(2):155–158, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [GDF⁺04] **Gomez:2004:EFT**
M. E. Gomez, J. Duato, J. Flich, P. Lopez, A. Robles, N. A. Nordbotten, O. Lysne, and T. Skeie. An efficient fault-tolerant routing methodology for meshes and tori. *IEEE Computer Architecture Letters*, 3(1):3, January 2004. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [GDU⁺24] **Gohil:2024:IGM**
Varun Gohil, Sundar Dev, Gaurang Upasani, David Lo, Parthasarathy Ranganathan, and Christina Delimitrou. The importance of generalizability in machine learning for systems. *IEEE Computer Architecture Letters*, 23(1):95–98, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [GF16] **Gorgues:2016:EPC**
Miguel Gorgues and Jose Flich. End-point congestion filter for adaptive routing with congestion-insensitive performance. *IEEE Computer Architecture Letters*, 15(1):9–12, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [GFAHSA24] **Gheibi-Fetrat:2024:TTF**
Atiyeh Gheibi-Fetrat, Negar Akbarzadeh, Shaahin Hessabi, and Hamid Sarbazi-Azad. Tulip: Turn-free low-power network-on-chip. *IEEE Computer Architecture Letters*, 23(1):5–8, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [GG11] **Gou:2011:ESH**
Chunyang Gou and Georgi N. Gaydadjiev. Exploiting SPMD horizontal locality. *IEEE Computer Architecture Letters*, 10(1):20–23, January/June 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [GG17] **Garland:2017:LCM**
James Garland and David Gregg. Low complexity multiply accumulate unit for weight-sharing convolutional

- neural networks. *IEEE Computer Architecture Letters*, 16(2):132–135, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [GJ21]
- [GGM⁺16] P. Garcia, T. Gomes, J. Monteiro, A. Tavares, and M. Ekpanyapong. On-chip message passing sub-system for embedded inter-domain communication. *IEEE Computer Architecture Letters*, 15(1):33–36, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [GGS19] H. Golestani, G. Gupta, and R. Sen. Performance modeling and bottleneck analysis of EDGE processors using dependence graphs. *IEEE Computer Architecture Letters*, 18(1):79–82, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [GKKW07]
- [GIH⁺24] Courtney Golden, Dan Ilan, Caroline Huang, Niansong Zhang, Zhiru Zhang, and Christopher Batten. Supporting a virtual vector instruction set on a commercial compute-in-SRAM accelerator. *IEEE Computer Architecture Letters*, 23(1):29–32, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic). [GLH⁺20]
- [Ghasemi:2021:MPE] Fatemeh Ghasemi and Magnus Jahre. Modeling periodic energy-harvesting computing systems. *IEEE Computer Architecture Letters*, 20(2):142–145, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Gouk:2022:PHA] Donghyun Gouk, Seungkwan Kang, Miryeong Kwon, Junhyeok Jang, Hyunkyoo Choi, Sangwon Lee, and Myoungsoo Jung. PreGNN: Hardware acceleration to take pre-processing off the critical path in graph neural networks. *IEEE Computer Architecture Letters*, 21(2):117–120, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Guz:2007:NCO] Z. Guz, I. Keidar, A. Kolodny, and U. Weiser. Nahalal: Cache organization for chip multiprocessors. *IEEE Computer Architecture Letters*, 6(1):21–24, January 2007. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Gu:2020:NTC] Peng Gu, Benjamin S. Lim, Wenqin Huangfu, Krishan T. Malladi, Andrew Chang,

and Yuan Xie. NMTSim: Transaction-command based simulator for new memory technology devices. *IEEE Computer Architecture Letters*, 19(1):76–79, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).

Gurumurthi:2021:HRE

[GLJ⁺21]

Sudhanva Gurumurthi, Kijun Lee, Munseon Jang, Vilas Sridharan, Aaron Nygren, Yesin Ryu, Kyomin Sohn, Taekyun Kim, and Hoeju Chung. HBM3 RAS: Enhancing resilience at scale. *IEEE Computer Architecture Letters*, 20(2):158–161, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).

Gupta:2019:DQL

[GMM⁺19]

Ujjwal Gupta, Sumit K. Mandal, Manqing Mao, Chaitali Chakrabarti, and Umit Y. Ogras. A deep Q-learning approach for dynamic management of heterogeneous processors. *IEEE Computer Architecture Letters*, 18(1):14–17, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Gibert:2015:PSR

[GMMC15]

Enric Gibert, Raul Martínez, Carlos Madriles, and Josep M. Codina. Profiling support for runtime managed code: Next generation performance mon-

itoring units. *IEEE Computer Architecture Letters*, 14(1):62–65, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Garcia-Mallen:2023:TAD

[GMPMC⁺23]

Jonathan Garcia-Mallen, Shuo-hao Ping, Alex Miralles-Cordal, Ian Martin, Mukund Ramakrishnan, and Yipeng Huang. Towards an accelerator for differential and algebraic equations useful to scientists. *IEEE Computer Architecture Letters*, 22(2):185–188, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).

Gupta:2015:CEO

[GO15]

Ujjwal Gupta and Umit Y. Ogras. Constrained energy optimization in heterogeneous platforms using generalized scaling models. *IEEE Computer Architecture Letters*, 14(1):21–25, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Gaudiot:2006:F

[GPS06]

J.-L. Gaudiot, Y. Patt, and K. Skadon. Foreword. *IEEE Computer Architecture Letters*, 5(1):11, January 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [GQLZ19] **Gan:2019:SSV**
 Yiming Gan, Yuxian Qiu, Jingwen Leng, and Yuhao Zhu. SVSoC: Speculative vision systems-on-a-chip. *IEEE Computer Architecture Letters*, 18(1):47–50, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [GRCV02] **Gordon-Ross:2002:EFP**
 A. Gordon-Ross, S. Cotterell, and F. Vahid. Exploiting fixed programs in embedded systems: a loop cache example. *IEEE Computer Architecture Letters*, 1(1):2, January 2002. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [GSG⁺17] **Gottscho:2017:MIM**
 Mark Gottscho, Mohammed Shoaib, Sriram Govindan, Bikash Sharma, Di Wang, and Puneet Gupta. Measuring the impact of memory errors on application performance. *IEEE Computer Architecture Letters*, 16(1):51–55, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [GVG⁺08] **GomezRequena:2008:BFT**
 C. Gomez Requena, F. Gilabert Villamon, M. Gomez, P. Lopez, and J. Duato. Beyond fat-tree: Unidirectional load-balanced multistage interconnection network. *IEEE Computer Architecture Letters*, 7(2):49–52, July 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). See comment [Ant09].
- [GWR08] **Golander:2008:DDS**
 A. Golander, S. Weiss, and R. Ronen. DDMR: Dynamic and scalable dual modular redundancy with short validation intervals. *IEEE Computer Architecture Letters*, 7(2):65–68, July 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [HA24] **Hafezan:2024:IEE**
 Mohammad Hafezan and Ehsan Atoofian. Improving energy-efficiency of capsule networks on modern GPUs. *IEEE Computer Architecture Letters*, 23(1):49–52, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [HBL⁺10] **Hoang:2010:CAN**
 Giang Hoang, Chang Bae, John Lange, Lide Zhang, Peter Dinda, and Russ Joseph. A case for alternative nested paging models for virtualized systems. *IEEE Computer Architecture Letters*, 9(1):17–20, January/June 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [HBW⁺23] **Hossain:2023:SDA**
 Naorin Hossain, Alper Buyuktosunoglu, John-David Well-

- man, Pradip Bose, and Margaret Martonosi. SoCurity: a design approach for enhancing SoC security. *IEEE Computer Architecture Letters*, 22(2):105–108, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic). [HDAS18]
- [HCK⁺21] Hyungkyu Ham, Hyunuk Cho, Minjae Kim, Jueon Park, Jeongmin Hong, Hyojin Sung, Eunhyeok Park, Euicheol Lim, and Gwangsun Kim. Near-data processing in memory expander for DNN acceleration on GPUs. *IEEE Computer Architecture Letters*, 20(2):171–174, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic). [HEDH21]
- [HCK22] Jeongmin Hong, Sungjun Cho, and Gwangsun Kim. Overcoming memory capacity wall of GPUs with heterogeneous memory stack. *IEEE Computer Architecture Letters*, 21(2):61–64, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic). [HH22]
- [HCM10] Mohammad Hammoud, Sangyeun Cho, and Rami G. Melhem. A dynamic pressure-aware associative placement strategy for large scale chip multiprocessors. *IEEE Computer Architecture Letters*, 9(1):29–32, January/June 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Hadjilambrou:2018:SCV]
- Zacharias Hadjilambrou, Shidhartha Das, Marco A. Antoniadis, and Yiannakis Sazeides. Sensing CPU voltage noise through electromagnetic emanations. *IEEE Computer Architecture Letters*, 17(1):68–71, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Heirman:2021:RRC]
- Wim Heirman, Stijn Eyerman, Kristof Du Bois, and Ibrahim Hur. RIO: RO-centric in-order modeling of out-of-order processors. *IEEE Computer Architecture Letters*, 20(1):78–81, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic). [Huang:2022:EDC]
- Jianming Huang and Yu Hua. Ensuring data confidentiality in eADR-Based NVM systems. *IEEE Computer Architecture Letters*, 21(2):153–156, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic). [Hameed:2022:DPA]
- Fazal Hameed, Asif Ali Khan, Sebastien Ollivier, Alex K.

- Jones, and Jeronimo Castrillon. DNA pre-alignment filter using processing near race-track memory. *IEEE Computer Architecture Letters*, 21(2):53–56, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Hos18] Morteza Hoseinzadeh. Flow-based simulation methodology. *IEEE Computer Architecture Letters*, 17(1):51–54, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [HLH16] Qi Hu, Peng Liu, and Michael C. Huang. Threads and data mapping: Affinity analysis for traffic reduction. *IEEE Computer Architecture Letters*, 15(2):133–136, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [HPS23] Adam Hastings, Ryan Piersma, and Simha Sethumadhavan. Architectural security regulation. *IEEE Computer Architecture Letters*, 22(2):173–176, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [HLR21] Bongjoon Hyun, Jiwon Lee, and Minsoo Rhu. Characterization and analysis of deep learning for 3D point cloud analytics. *IEEE Computer Architecture Letters*, 20(2):106–109, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [HR10] Andrew Hilton and Amir Roth. SMT-Directory: Efficient load-load ordering for SMT. *IEEE Computer Architecture Letters*, 9(1):25–28, January/June 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [HMCP16] Milad Hashemi, Debbie Marr, Doug Carmean, and Yale N. Patt. Efficient execution of bursty applications. *IEEE Computer Architecture Letters*, 15(2):85–88, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [HRF⁺11] Carles Hernandez, Antoni Roca, Jose Flich, Federico Silla, and Jose Duato. Fault-tolerant vertical link design for effective 3D stacking. *IEEE Computer Architecture Letters*, 10(2):41–44, July/December 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Hoseinzadeh:2018:FBS**Hu:2016:TDM****Hastings:2023:ASR****Hyun:2021:CAD****Hilton:2010:SDE****Hashemi:2016:EEB****Hernandez:2011:FTV**

- [HS04] **Holloway:2004:CPS**
A. L. Holloway and G. S. Sohi. Characterization of problem stores. *IEEE Computer Architecture Letters*, 3(1):9, January 2004. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [HSUS11] **Ho:2011:EIB**
Chen-Han Ho, Garret Staus, Aaron Ulmer, and Karthikeyan Sankaralingam. Exploring the interaction between device lifetime reliability and security vulnerabilities. *IEEE Computer Architecture Letters*, 10(2):37–40, July/December 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [HXL⁺22] **Hou:2022:CUE**
Xiaofeng Hou, Cheng Xu, Jiacheng Liu, Xuehan Tang, Lingyu Sun, Chao Li, and Kwang-Ting Cheng. Characterizing and understanding end-to-end multi-modal neural networks on GPUs. *IEEE Computer Architecture Letters*, 21(2):125–128, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [IKW⁺20] **Im:2020:PBA**
Junsu Im, Hanbyeol Kim, Yumin Won, Jiho Oh, Minjae Kim, and Sungjin Lee. Probability-based address translation for flash SSDs. *IEEE Computer Architecture Letters*, 19(2):97–100, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [ILG10] **Iqbal:2010:POS**
Syed Muhammad Zeeshan Iqbal, Yuchen Liang, and Hakan Grahn. ParMiBench — an open-source benchmark for embedded multiprocessor systems. *IEEE Computer Architecture Letters*, 9(2):45–48, July/December 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [ILNS20] **Ishii:2020:RIP**
Yasuo Ishii, Jaekyu Lee, Krishnendra Nathella, and Dam Sunwoo. Rebasng instruction prefetching: an industry perspective. *IEEE Computer Architecture Letters*, 19(2):147–150, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [ILXY18a] **Ipek:2018:BLL**
Engin Ipek, Florian Longnos, Shihai Xiao, and Wei Yang. Bit-level load balancing: a new technique for improving the write throughput of deeply scaled STT-MRAM. *IEEE Computer Architecture Letters*, 17(2):139–142, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [ILXY18b] Engin Ipek, Florian Longnos, Shihai Xiao, and Wei Yang. Vertical writes: Closing the throughput gap between deeply scaled STT-MRAM and DRAM. *IEEE Computer Architecture Letters*, 17(2):151–154, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Jac16a] Bruce Jacob. The 2 PetaFLOP, 3 petabyte, 9 TB/s, 90 kW cabinet: a system architecture for exascale and big data. *IEEE Computer Architecture Letters*, 15(2):125–128, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [IPS14] Aleksandar Ilic, Frederico Pratas, and Leonel Sousa. Cache-aware roofline model: Upgrading the loft. *IEEE Computer Architecture Letters*, 13(1):21–24, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [IXS18] Konstantinos Iliakis, Sotirios Xydis, and Dimitrios Soudris. Decoupled MapReduce for shared-memory multi-core architectures. *IEEE Computer Architecture Letters*, 17(2):143–146, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [IXS19] Konstantinos Iliakis, Sotirios Xydis, and Dimitrios Soudris. LOOG: Improving GPU efficiency with light-weight out-of-order execution. *IEEE Computer Architecture Letters*, 18(2):166–169, July 2019. ISSN 1556-6064.
- [JAC16] Bruce Jacob. The 2 PetaFLOP, 3 petabyte, 9 TB/s, 90 kW cabinet: a system architecture for exascale and big data. *IEEE Computer Architecture Letters*, 15(2):125–128, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [JAM17] Patrick Judd, Jorge Albericio, and Andreas Moshovos. Stripes: Bit-serial deep neural network computing. *IEEE Computer Architecture Letters*, 16(1):80–83, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [JC17] Dong-Ik Jeon and Ki-Seok Chung. CasHMC: a cycle-accurate simulator for hybrid memory cube. *IEEE Computer Architecture Letters*, 16(1):10–13, January/

June 2017. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).

Juang:2002:IDT

[JDK⁺02]

Philo Juang, P. Diodato, S. Kaxiras, K. Skadron, Zhigang Hu, M. Martonosi, and D. W. Clark. Implementing decay techniques using 4T quasi-static memory cells. *IEEE Computer Architecture Letters*, 1(1):10, January 2002. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).

Jalili:2022:MPD

[JE22]

Majid Jalili and Mattan Erez. Managing prefetchers with deep reinforcement learning. *IEEE Computer Architecture Letters*, 21(2):105–108, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).

Jeon:2019:LAG

[JEAG⁺19]

Hyeran Jeon, Hodjat Asghari Esfeden, Nael B. Abu-Ghazaleh, Daniel Wong, and Sindhuja Elango. Locality-aware GPU register file. *IEEE Computer Architecture Letters*, 18(2):153–156, July 2019. ISSN 1556-6064.

Jin:2022:MPC

[JJP⁺22]

Hoyong Jin, Donghun Jeong, Taewon Park, Jong Hwan Ko, and Jungrae Kim. Multi-prediction compression: an efficient and scalable memory

compression framework for GP-GPU. *IEEE Computer Architecture Letters*, 21(2):37–40, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).

Jang:2021:DPT

[JKK⁺21]

Yongjoo Jang, Sejin Kim, Daehoon Kim, Sungjin Lee, and Jaeha Kung. Deep partitioned training from near-storage computing to DNN accelerators. *IEEE Computer Architecture Letters*, 20(1):70–73, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).

Jung:2016:LPS

[JLA16]

Daejin Jung, Sheng Li, and Jung Ho Ahn. Large pages on steroids: Small ideas to accelerate big memory applications. *IEEE Computer Architecture Letters*, 15(2):101–104, July/December 2016. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).

Jeon:2023:HAR

[JLKK23]

Kiseok Jeon, Junghee Lee, Bumsoo Kim, and James J. Kim. Hardware accelerated reusable Merkle tree generation for bitcoin blockchain headers. *IEEE Computer Architecture Letters*, 22(2):69–72, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).

- [JLP07] **Jerger:2007:CSC**
N. Enright Jerger, M. Lipasti, and L. Peh. Circuit-switched coherence. *IEEE Computer Architecture Letters*, 6(1):5–8, January 2007. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [JLRA18] **Jung:2018:PCU**
Daejin Jung, Sunjung Lee, Wonjong Rhee, and Jung Ho Ahn. Partitioning compute units in CNN acceleration for statistical memory traffic shaping. *IEEE Computer Architecture Letters*, 17(1):72–75, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [JLS⁺23] **Jeong:2023:LLA**
Ipoom Jeong, Jiaqi Lou, Yongseok Son, Yongjoo Park, Yifan Yuan, and Nam Sung Kim. LADIO: Leakage-aware direct I/O for I/O-intensive workloads. *IEEE Computer Architecture Letters*, 22(2):77–80, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [JMKP07] **Joao:2007:DPI**
J. A. Joao, O. Mutlu, H. Kim, and Y. N. Patt. Dynamic predication of indirect jumps. *IEEE Computer Architecture Letters*, 6(2):25–28, February 2007. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [JMKP08] **Joao:2008:DPI**
J. A. Joao, O. Mutlu, H. Kim, and Y. N. Patt. Dynamic predication of indirect jumps. *IEEE Computer Architecture Letters*, 7(1):1–4, January 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [JP13] **Joo:2013:HPS**
Yongsoo Joo and Sangsoo Park. A hybrid PRAM and STT-RAM cache architecture for extending the lifetime of PRAM caches. *IEEE Computer Architecture Letters*, 12(2):55–58, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [JPC18] **Jeon:2018:HMP**
Dong-Ik Jeon, Kyeong-Bin Park, and Ki-Seok Chung. HMC-MAC: Processing-in-memory architecture for multiply-accumulate operations with hybrid memory cube. *IEEE Computer Architecture Letters*, 17(1):5–8, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [JSDK13] **Jian:2013:HPE**
Xun Jian, John Sartori, Henry Duwe, and Rakesh Kumar. High performance, energy efficient chipkill correct memory with multidimensional parity. *IEEE Computer*

- Architecture Letters*, 12(2): 39–42, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [JY24]
- Jahanshahi:2020:GNC**
- [JSLW20] Ali Jahanshahi, Hadi Zamani Sabzi, Chester Lau, and Daniel Wong. GPU-NEST: Characterizing energy efficiency of multi-GPU inference servers. *IEEE Computer Architecture Letters*, 19(2):139–142, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Jimenez:2023:LLC**
- [JTG23] Daniel A. Jiménez, Elvira Teran, and Paul V. Gratz. Last-level cache insertion and promotion policy in the presence of aggressive prefetching. *IEEE Computer Architecture Letters*, 22(1):17–20, January/June 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Jung:2017:NIP**
- [Jun17] Myoungsoo Jung. NearZero: an integration of phase change memory with multi-core coprocessor. *IEEE Computer Architecture Letters*, 16(2):136–140, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Jahshan:2024:MMB**
- Z. Jahshan and L. Yavits. MajorK: Majority based kmer matching in commodity DRAM. *IEEE Computer Architecture Letters*, 23(1): 83–86, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Jung:2018:SMS**
- [JZA⁺18] Myoungsoo Jung, Jie Zhang, Ahmed Abulila, Miryeong Kwon, Narges Shahidi, John Shalf, Nam Sung Kim, and Mahmut Kandemir. SimpleSSD: Modeling solid state drives for holistic system simulation. *IEEE Computer Architecture Letters*, 17(1):37–41, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Kim:2007:FBT**
- [KBD07] J. Kim, J. Balfour, and W. J. Dally. Flattened butterfly topology for on-chip networks. *IEEE Computer Architecture Letters*, 6(2):37–40, February 2007. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Kumar:2020:PSM**
- [KCB⁺20] Chanchal Kumar, Aayush Chaudhary, Shubham Bhawalkar, Utkarsh Mathur, Saransh Jain, Adith Vastrad, and Eric Rotenberg. Post-silicon microarchitecture. *IEEE Computer Architecture Letters*,

- 19(1):26–29, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic). [KDS22]
- [KCP+19] Jiho Kim, Jehoo Cha, Jason Jong Kyu Park, Dong-suk Jeon, and Yongjun Park. Improving GPU multitasking efficiency using dynamic resource sharing. *IEEE Computer Architecture Letters*, 18(1):1–5, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [KDJ+03]
- [KCPG18] Manolis Kaliorakis, Athanasios Chatzidimitriou, George Papadimitriou, and Dimitris Gizopoulos. Statistical analysis of multicore CPUs operation in scaled voltage conditions. *IEEE Computer Architecture Letters*, 17(2):109–112, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [KG10]
- [KDL23] Soroosh Khoram, Kyle Daruwalla, and Mikko Lipasti. Energy-efficient Bayesian inference using bitstream computing. *IEEE Computer Architecture Letters*, 22(1):37–40, January/June 2023. ISSN 1556-6056 (print), 1556-6064 (electronic). [KH18]
- [Kokkinis:2022:DOC] Argyris Kokkinis, Dionysios Diamantopoulos, and Kostas Siozios. Dynamic optimization of on-chip memories for HLS targeting many-accelerator platforms. *IEEE Computer Architecture Letters*, 21(2):41–44, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Kumar:2003:PPR] R. Kumar, K. Farkas, N. P. Jouppi, P. Ranganathan, and D. M. Tullsen. Processor power reduction via single-ISA heterogeneous multi-core architectures. *IEEE Computer Architecture Letters*, 2(1):2, January 2003. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Kim:2010:LUC] Hyungjun Kim and Paul V. Gratz. Leveraging unused cache block words to reduce power in CMP interconnect. *IEEE Computer Architecture Letters*, 9(1):33–36, January/June 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Kondguli:2018:BUS] Sushant Kondguli and Michael Huang. Bootstrapping: Using SMT hardware to improve single-thread performance. *IEEE Computer Ar-*

- chitecture Letters*, 17(2):205–208, July/December 2018. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic). [KJK21]
- Khan:2019:RCA**
- [KHB⁺19] Asif Ali Khan, Fazal Hameed, Robin Blasing, Stuart Parkin, and Jeronimo Castrillon. RT-Sim: a cycle-accurate simulator for racetrack memories. *IEEE Computer Architecture Letters*, 18(1):43–46, January/June 2019. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Khan:2024:EML**
- [KHS⁺24a] Asif Ali Khan, Fazal Hameed, Taha Shahroodi, Alex K. Jones, and Jeronimo Castrillon. Efficient memory layout for pre-alignment filtering of long DNA reads using race-track memory. *IEEE Computer Architecture Letters*, 23(1):129–132, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic). [KK21]
- Kim:2024:ADR**
- [KHS⁺24b] Yang-Gon Kim, Yun-Ki Han, Jae-Kang Shin, Jun-Kyum Kim, and Lee-Sup Kim. Accelerating deep reinforcement learning via phase-level parallelism for robotics applications. *IEEE Computer Architecture Letters*, 23(1):41–44, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Kim:2021:DSR**
- Jiho Kim, Myoungsoo Jung, and John Kim. Decoupled SSD: Reducing data movement on NAND-based flash SSD. *IEEE Computer Architecture Letters*, 20(2):150–153, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Kim:2019:THA**
- [KJS⁺19] S. Kim, H. Jung, W. Shin, H. Lee, and H. Lee. HAD-TWL: Hot address detection-based wear leveling for phase-change memory systems with low latency. *IEEE Computer Architecture Letters*, 18(2):107–110, July 2019. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Kasan:2021:CDB**
- [KK21] Hans Kasan and John Kim. The case for dynamic bias in global adaptive routing. *IEEE Computer Architecture Letters*, 20(1):38–41, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Kim:2014:VPT**
- [KKH14] Daehoon Kim, Hwanju Kim, and Jaehyuk Huh. vCache: Providing a transparent view of the LLC in virtualized environments. *IEEE Computer Architecture Letters*, 13(2):109–112, July/December 2014. CODEN ????? ISSN

- 1556-6056 (print), 1556-6064 (electronic).
- [KKJ⁺22] **Kim:2022:SSE**
Sejin Kim, Jungwoo Kim, Yongjoo Jang, Jaeha Kung, and Sungjin Lee. SEMS: Scalable embedding memory system for accelerating embedding-based DNNs. *IEEE Computer Architecture Letters*, 21(2):157–160, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KKK13] **Kim:2013:CFC**
Hanjoon Kim, Yonggon Kim, and John Kim. Clumsy flow control for high-throughput bufferless on-chip networks. *IEEE Computer Architecture Letters*, 12(2):47–50, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KKKH18] **Kim:2018:ZRV**
Seikwon Kim, Wonsang Kwak, Changdae Kim, and Jaehyuk Huh. Zebra refresh: Value transformation for zero-aware DRAM refresh reduction. *IEEE Computer Architecture Letters*, 17(2):130–133, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KKL⁺07] **Kodakara:2007:CRM**
S. Kodakara, J. Kim, D. Lilja, D. Hawkins, W. Hsu, and P. Yew. CIM: a reliable metric for evaluating program phase classifications. *IEEE Computer Architecture Letters*, 6(1):9–12, January 2007. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KKL⁺15] **Kim:2015:PEM**
Seung Hun Kim, Dohoon Kim, Changmin Lee, Won Seob Jeong, Won Woo Ro, and Jean-Luc Gaudiot. A performance-energy model to evaluate single thread execution acceleration. *IEEE Computer Architecture Letters*, 14(2):99–102, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KKL20] **Kim:2020:TSA**
Minsub Kim, Jaeha Kung, and Sungjin Lee. Towards scalable analytics with inference-enabled solid-state drives. *IEEE Computer Architecture Letters*, 19(1):13–17, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KKL⁺23] **Kim:2023:HAC**
Yonghae Kim, Anurag Kar, Jaewon Lee, Jaekyu Lee, and Hyesoon Kim. Hardware-assisted code-pointer tagging for forward-edge control-flow integrity. *IEEE Computer Architecture Letters*, 22(2):117–120, July/December 2023.

- ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KKLL22] **Kim:2022:CSD** Minjae Kim, Bryan S. Kim, Eunji Lee, and Sungjin Lee. A case study of a DRAM-NVM hybrid memory allocator for key-value stores. *IEEE Computer Architecture Letters*, 21(2):81–84, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KPP⁺18] **Kim:2018:SPM** Jihun Kim, Joonsung Kim, Pyeongsu Park, Jong Kim, and Jangwoo Kim. SSD performance modeling using bottleneck analysis. *IEEE Computer Architecture Letters*, 17(1):80–83, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KL02] **KleinOsowski:2002:MNS** A. J. KleinOsowski and D. J. Lilja. MinneSPEC: a new SPEC benchmark workload for simulation-based computer architecture research. *IEEE Computer Architecture Letters*, 1(1):7, January 2002. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KL18] **Kim:2018:HBP** Chinam Kim and Hyukjun Lee. A high-bandwidth PCM-based memory system for highly available IP routing table lookup. *IEEE Computer Architecture Letters*, 17(2):246–249, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KLCA21] **Kim:2021:RSD** Hweesoo Kim, Sunjung Lee, Jaewan Choi, and Jung Ho Ahn. Row-streaming dataflow using a chaining buffer and systolic array+ structure. *IEEE Computer Architecture Letters*, 20(1):34–37, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KLKK14] **Kim:2014:SGA** Youngsok Kim, Jaewon Lee, Donggyu Kim, and Jangwoo Kim. ScaleGPU: GPU architecture for memory-unaware GPU programming. *IEEE Computer Architecture Letters*, 13(2):101–104, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KLR24] **Kim:2024:FAD** Hyeseong Kim, Yunjae Lee, and Minsoo Rhu. FPGA-accelerated data preprocessing for personalized recommendation systems. *IEEE Computer Architecture Letters*, 23(1):7–10, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).

- [KLSD11] **Khan:2011:DDC**
 Omer Khan, Mieszko Lis, Yildiz Sinangil, and Srinivas Devadas. DCC: a dependable cache coherence multicore architecture. *IEEE Computer Architecture Letters*, 10(1): 12–15, January/June 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KLWJ21] **Kim:2021:ZCS**
 Sunghwan Kim, Gysun Lee, Jiwon Woo, and Jinkyu Jeong. Zero-copying I/O stack for low-latency SSDs. *IEEE Computer Architecture Letters*, 20(1):50–53, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KLZ12] **Kong:2012:ASF**
 Ji Kong, Peilin Liu, and Yu Zhang. Atomic streaming: a framework of on-chip data supply system for task-parallel MPSoCs. *IEEE Computer Architecture Letters*, 11(1):5–8, January/June 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KMJ18] **Kline:2018:CAR**
 Donald Kline, Jr., Rami Melhem, and Alex K. Jones. Counter advance for reliable encryption in phase change memory. *IEEE Computer Architecture Letters*, 17(2):209–212, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KNE+14] **Kvatinsky:2014:MBM**
 Shahar Kvatinsky, Yuval H. Nacson, Yoav Etsion, Eby G. Friedman, Avinoam Kolodny, and Uri C. Weiser. Memristor-based multithreading. *IEEE Computer Architecture Letters*, 13(1):41–44, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KNG+18] **Khatamifard:2018:MSD**
 S. Karen Khatamifard, M. Hassan Najafi, Ali Ghoreyshi, Ulya R. Karpuzcu, and David J. Lilja. On memory system design for stochastic computing. *IEEE Computer Architecture Letters*, 17(2):117–121, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KNGK15] **Kang:2015:SRT**
 Suk Chan Kang, Chrysostomos Nicopoulos, Ada Gavrilovska, and Jongman Kim. Subtleties of run-time virtual address stacks. *IEEE Computer Architecture Letters*, 14(2):152–155, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [KNQ15] **Kim:2015:ASM**
Dae-Hyun Kim, Prashant J. Nair, and Moinuddin K. Qureshi. Architectural support for mitigating row hammering in DRAM memories. *IEEE Computer Architecture Letters*, 14(1):9–12, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KPL⁺21] **Kalani:2021:ICB**
Neelu Shivprakash Kalani and Biswabandan Panda. Instruction criticality based energy-efficient hardware data prefetching. *IEEE Computer Architecture Letters*, 20(2):146–149, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KPPK21] **Krimer:2010:SNT**
Evgeni Krimer, Robert Pawlowski, Mattan Erez, and Patrick Chiang. Synctium: a near-threshold stream processor for energy-constrained parallel applications. *IEEE Computer Architecture Letters*, 9(1):21–24, January/June 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KQD18] **Kang:2020:NPP**
Ki-Dong Kang, Gyeongseo Park, Nam Sung Kim, and Daehoon Kim. Network packet processing mode-aware power management for data center servers. *IEEE Computer Architecture Letters*, 19(1):1–4, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KPL⁺21] **Kim:2021:TTR**
Byeongho Kim, Jaehyun Park, Eojin Lee, Minsoo Rhu, and Jung Ho Ahn. TRiM: Tensor reduction in memory. *IEEE Computer Architecture Letters*, 20(1):5–8, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KPPK21] **Kwon:2021:FQM**
Hyoukjun Kwon, Michael Pellauer, Angshuman Parashar, and Tushar Krishna. Flexion: a quantitative metric for flexibility in DNN accelerators. *IEEE Computer Architecture Letters*, 20(1):1–4, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KPEK10] **Kulkarni:2018:LAI**
Neeraj Kulkarni, Feng Qi, and Christina Delimitrou. Leveraging approximation to improve datacenter resource efficiency. *IEEE Computer Architecture Letters*, 17(2):171–174, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [KQGS16] **Kannan:2016:EAP** Sudarsun Kannan, Moinudin Qureshi, Ada Gavrilovska, and Karsten Schwan. Energy aware persistence: Reducing the energy overheads of persistent memory. *IEEE Computer Architecture Letters*, 15(2):89–92, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KR18] **Kwon:2018:CMC** Youngeun Kwon and Minsoo Rhu. A case for memory-centric HPC system architecture for training deep neural networks. *IEEE Computer Architecture Letters*, 17(2):134–138, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KRB⁺13] **Karsli:2013:EDT** I. Burak Karsli, Pedro Reviriego, M. Fatih Balli, Oğuz Ergin, and J. A. Maestro. Enhanced duplication: a technique to correct soft errors in narrow values. *IEEE Computer Architecture Letters*, 12(1):13–16, January/June 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KSB19] **Kumar:2019:HRA** Chanchal Kumar, Sidharth Singh, and Gregory T. Byrd. Hybrid remote access proto-
- col. *IEEE Computer Architecture Letters*, 18(1):30–33, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KSO⁺16] **Kleanthous:2016:TML** Marios Kleanthous, Yiannakis Sazeides, Emre Ozer, Chrysostomos Nicopoulos, Panagiota Nikolaou, and Zacharias Hadjilambrou. Toward multi-layer holistic evaluation of system designs. *IEEE Computer Architecture Letters*, 15(1):58–61, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KWB⁺20] **Krishnan:2020:SLV** Srivatsan Krishnan, Zishen Wan, Kshitij Bhardwaj, Paul Whatmough, Aleksandra Faust, Gu-Yeon Wei, David Brooks, and Vijay Janapa Reddi. The sky is not the limit: a visual performance model for cyber-physical co-design in autonomous machines. *IEEE Computer Architecture Letters*, 19(1):38–42, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [KWKK18] **Khatamifard:2018:NCC** S. Karen Khatamifard, Longfei Wang, Selcuk Köse, and Ulya R. Karpuzcu. A new class of covert channels exploiting power management

- vulnerabilities. *IEEE Computer Architecture Letters*, 17(2):201–204, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [KYP21]
- [KWL13] Yi Kai, Yi Wang, and Bin Liu. GreenRouter: Reducing power by innovating router’s architecture. *IEEE Computer Architecture Letters*, 12(2):51–54, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). **Kai:2013:GRP**
- [KWL⁺17] Samira Khan, Chris Wilkerson, Donghyuk Lee, Alaa R. Alameldeen, and Onur Mutlu. A case for memory content-based detection and mitigation of data-dependent failures in DRAM. *IEEE Computer Architecture Letters*, 16(2):88–93, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). **Khan:2017:CMC**
- [KYM16] Yoongu Kim, Weikun Yang, and Onur Mutlu. Ramulator: a fast and extensible DRAM simulator. *IEEE Computer Architecture Letters*, 15(1):45–49, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). **Kim:2016:RFE**
- [KZY⁺19] Vamsee Reddy Kommareddy, Baogang Zhang, Fan Yao, Rickard Ewetz, and Amro Awad. Are crossbar memories secure? New security vul- **Kommareddy:2019:CMS**
- Pratik Kumar, Chavhan Sajeet Yashavant, and Biswabandan Panda. DAMARU: a denial-of-service attack on randomized last-level caches. *IEEE Computer Architecture Letters*, 20(2):138–141, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic). **Kumar:2021:DDS**
- [KYW⁺24] Hyungyo Kim, Gaohan Ye, Nachuan Wang, Amir Yazdanbakhsh, and Nam Sung Kim. Exploiting Intel Advanced Matrix Extensions (AMX) for large language model inference. *IEEE Computer Architecture Letters*, 23(1):117–120, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic). **Kim:2024:EIA**
- [KZL18] Soroosh Khoram, Yue Zha, and Jing Li. An alternative analytical approach to associative processing. *IEEE Computer Architecture Letters*, 17(2):113–116, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). **Khoram:2018:AAA**

- nerabilities in crossbar memories. *IEEE Computer Architecture Letters*, 18(2):174–177, July 2019. ISSN 1556-6064. [LAS22]
- [LA16] Dongdong Li and Tor M. Aamodt. Inter-core locality aware memory scheduling. *IEEE Computer Architecture Letters*, 15(1):25–28, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [LAX+20]
- [LAC14] Maysam Lavasani, Hari Angepat, and Derek Chiou. An FPGA-based in-line accelerator for Memcached. *IEEE Computer Architecture Letters*, 13(2):57–60, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [LBB+19]
- [LAM+22] Benjamin J. Lucas, Ali Alwan, Marion Murzello, Yazheng Tu, Pengzhou He, Andrew J. Schwartz, David Guevara, Ujjwal Guin, Kyle Juretus, and Jiafeng Xie. Lightweight hardware implementation of binary ring-LWE PQC accelerator. *IEEE Computer Architecture Letters*, 21(1):17–20, January/June 2022. ISSN 1556-6056 (print), 1556-6064 (electronic). [LCHL20]
- Lenjani:2022:PAH**
Marzieh Lenjani, Alif Ahmed, and Kevin Skadron. Pulley: an algorithm/hardware co-optimization for in-memory sorting. *IEEE Computer Architecture Letters*, 21(2):109–112, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Lazarev:2020:DTE**
Nikita Lazarev, Neil Adit, Shaojie Xiang, Zhiru Zhang, and Christina Delimitrou. Dagger: Towards efficient RPCs in cloud microservices with near-memory reconfigurable NICs. *IEEE Computer Architecture Letters*, 19(2):134–138, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Leng:2019:ARA**
J. Leng, A. Buyuktosunoglu, R. Bertran, P. Bose, and V. J. Reddi. Asymmetric resilience for accelerator-rich systems. *IEEE Computer Architecture Letters*, 18(1):83–86, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Lai:2020:TDB**
Bo-Cheng Lai, Chun-Yen Chen, Yi-Da Hsin, and Bo-Yen Lin. A two-directional BigData sorting architecture on FPGAs. *IEEE Computer*

- Architecture Letters*, 19(1):72–75, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic). [LEBM20]
- [LCKA23] Hailong Li, Jaewan Choi, Yongsuk Kwon, and Jung Ho Ahn. A hardware-friendly tiled singular-value decomposition-based matrix multiplication for transformer-based models. *IEEE Computer Architecture Letters*, 22(2):169–172, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic). [LG20]
- [LCW⁺16] Minghua Li, Guancheng Chen, Qijun Wang, Yonghua Lin, Peter Hofstee, Per Stenstrom, and Dian Zhou. PATER: a hardware prefetching automatic tuner on IBM POWER8 processor. *IEEE Computer Architecture Letters*, 15(1):37–40, January/June 2016. CODEN ??? ISSN 1556-6056 (print), 1556-6064 (electronic). [LGLK17]
- [LCW⁺24] Tianzheng Li, Enfang Cui, Yuting Wu, Qian Wei, and Yue Gao. TeleVM: a lightweight virtual machine for RISC-V architecture. *IEEE Computer Architecture Letters*, 23(1):121–124, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic). [LHCK22]
- Lachtar:2020:CSA**
Nada Lachtar, Abdulrahman Abu Elkhail, Anys Bacha, and Hafiz Malik. A cross-stack approach towards defending against cryptojacking. *IEEE Computer Architecture Letters*, 19(2):126–129, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Li:2023:HFT**
- Li:2020:CDE**
Congmiao Li and Jean-Luc Gaudiot. Challenges in detecting an evasive spectre. *IEEE Computer Architecture Letters*, 19(1):18–21, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Li:2016:PHP**
- Lee:2017:FFE**
Junghee Lee, Kalidas Ganesh, Hyuk-Jun Lee, and Youngjae Kim. FESSD: a fast encrypted SSD employing on-chip access-control memory. *IEEE Computer Architecture Letters*, 16(2):115–118, July/December 2017. CODEN ??? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Li:2024:TLV**
- Lee:2022:MES**
Dusol Lee, Duwon Hong, Wonil Choi, and Jihong Kim. MQSim-E: an enterprise SSD simulator. *IEEE Computer Architecture Letters*, 21(1):13–16, January/June 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).

- [LHE⁺21] **Liu:2021:SMS** Wenjie Liu, Wim Heirman, Stijn Eyerman, Shoaib Akram, and Lieven Eeckhout. Scale-model simulation. *IEEE Computer Architecture Letters*, 20(2):175–178, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LHPR23] **Lee:2023:HHF** Seonho Lee, Ranggi Hwang, Jongse Park, and Minsoo Rhu. HAMMER: Hardware-friendly approximate computing for self-attention with mean-redistribution and linearization. *IEEE Computer Architecture Letters*, 22(1):13–16, January/June 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LHWB10] **Lyons:2010:ASF** Michael J. Lyons, Mark Hempstead, Gu-Yeon Wei, and David Brooks. The accelerator store framework for high-performance, low-power accelerator-based systems. *IEEE Computer Architecture Letters*, 9(2):53–56, July/December 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LHZ19] **Liu:2019:UFT** He Liu, Jianhui Han, and Youhui Zhang. A unified framework for training, mapping and simulation of ReRAM-based convolutional neural network acceleration. *IEEE Computer Architecture Letters*, 18(1):63–66, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LJ04] **Luo:2004:EES** Yue Luo and L. K. John. Efficiently evaluating speedup using sampled processor simulation. *IEEE Computer Architecture Letters*, 3(1):6, January 2004. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LJ18] **Lou:2018:BSB** Qian Lou and Lei Jiang. BRAWL: a spintronics-based portable basecalling-in-memory architecture for nanopore genome sequencing. *IEEE Computer Architecture Letters*, 17(2):239–242, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LJM⁺14] **Liu:2014:PTE** Qixiao Liu, Victor Jimenez, Miquel Moreto, Jaume Abella, Francisco J. Cazorla, and Mateo Valero. Per-task energy accounting in computing systems. *IEEE Computer Architecture Letters*, 13(2):85–88, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [LKA15] **Lee:2015:RDA**
Sungjin Lee, Jihong Kim, and Arvind. Refactored design of I/O architecture for flash storage. *IEEE Computer Architecture Letters*, 14(1):70–74, January/June 2015. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LKK19] **Lee:2019:ELM**
Seunghak Lee, Nam Sung Kim, and Daehoon Kim. Exploiting OS-level memory of-filing for DRAM power management. *IEEE Computer Architecture Letters*, 18(2):141–144, July 2019. ISSN 1556-6064.
- [LKKS15] **Lee:2015:SSI**
Junghee Lee, Youngjae Kim, Jongman Kim, and Galen M. Shipman. Synchronous I/O scheduling of independent write caches for an array of SSDs. *IEEE Computer Architecture Letters*, 14(1):79–82, January/June 2015. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LKL+21] **Lee:2021:LPM**
Hyeon Gyu Lee, Minwook Kim, Juwon Lee, Eunji Lee, Bryan S. Kim, Sungjin Lee, Yeseong Kim, Sang Lyul Min, and Jin-Soo Kim. Learned performance model for SSD. *IEEE Computer Architecture Letters*, 20(2):154–157, July/
- [LKP+23] **Lee:2023:NPR**
Seunghak Lee, Ki-Dong Kang, Gyeongseo Park, Nam Sung Kim, and Daehoon Kim. No-Hammer: Preventing row hammer with last-level cache management. *IEEE Computer Architecture Letters*, 22(2):157–160, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LKR21] **Lee:2021:UIN**
Yunjae Lee, Youngeun Kwon, and Minsoo Rhu. Understanding the implication of non-volatile memory for large-scale graph neural network training. *IEEE Computer Architecture Letters*, 20(2):118–121, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LLD+18] **Li:2018:BSB**
Zhaoshi Li, Leibo Liu, Yangdong Deng, Shouyi Yin, and Shaojun Wei. Breaking the synchronization bottleneck with reconfigurable transactional execution. *IEEE Computer Architecture Letters*, 17(2):147–150, July/December 2018. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).

- [LLJK23] **Lee:2023:CDC**
Hwanjun Lee, Seunghak Lee, Yeji Jung, and Daehoon Kim. T-CAT: Dynamic cache allocation for tiered memory systems with memory interleaving. *IEEE Computer Architecture Letters*, 22(2):73–76, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LLKS12] **Lakshminarayana:2012:DSP**
Nagesh B. Lakshminarayana, Jaekyu Lee, Hyesoon Kim, and Jinwoo Shin. DRAM scheduling policy for GPGPU architectures based on a potential function. *IEEE Computer Architecture Letters*, 11(2):33–36, July/December 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LLLM06] **Lee:2006:ASC**
Moon-Sang Lee, Sang-Kwon Lee, Joonwon Lee, and Seung-Ryoul Maeng. Adopting system call based address translation into user-level communication. *IEEE Computer Architecture Letters*, 5(1):26–29, January 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LLM⁺21] **Li:2021:RRA**
Qian Li, Bin Li, Pietro Mercati, Ramesh Illikkal, Charlie Tai, Michael Kishinevsky, and Christos Kozyrakis. RAMBO: Resource allocation for microservices using Bayesian optimization. *IEEE Computer Architecture Letters*, 20(1):46–49, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LLPC19] **Lin:2019:DSE**
Ting-Ru Lin, Yunfan Li, Masoud Pedram, and Lizhong Chen. Design space exploration of memory controller placement in throughput processors with deep learning. *IEEE Computer Architecture Letters*, 18(1):51–54, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LLS⁺15] **Liu:2015:LHP**
Longjun Liu, Chao Li, Hongbin Sun, Yang Hu, Jingmin Xin, Nanning Zheng, and Tao Li. Leveraging heterogeneous power for improving datacenter efficiency and resiliency. *IEEE Computer Architecture Letters*, 14(1):41–45, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LLSA18] **Lee:2018:TTW**
Eojin Lee, Sukhan Lee, G. Edward Suh, and Jung Ho Ahn. TWiCe: Time window counter based row refresh to prevent row-hammering. *IEEE Computer Architecture Letters*, 17(1):96–99, Jan-

- uary/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LMC⁺09] Carlos Luque, Miquel Moreto, Francisco J. Cazorla, Roberto Gioiosa, Alper Buyukto-sunoglu, and Mateo Valero. CPU accounting in CMP processors. *IEEE Computer Architecture Letters*, 8(1):17–20, January/June 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LMJ12] Yong Li, Rami Melhem, and Alex K. Jones. Leveraging sharing in second level translation-lookaside buffers for chip multiprocessors. *IEEE Computer Architecture Letters*, 11(2):49–52, July/December 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LMK06] W. Li, S. Mohanty, and K. Kavi. A page-based hybrid (software–hardware) dynamic memory allocator. *IEEE Computer Architecture Letters*, 5(2):13, February 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LMT⁺09] Jacob Leverich, Matteo Monchiero, Vanish Talwar, Partha Ranganathan, and Christos Kozyrakis. Power management of data-center workloads using per-core power gating. *IEEE Computer Architecture Letters*, 8(2):48–51, July/December 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LPK16] Bo-Cheng Charles Lai, Luis Garrido Platero, and Hsien-Kai Kuo. A quantitative method to data reuse patterns of SIMT applications. *IEEE Computer Architecture Letters*, 15(2):73–76, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LQYF23] Lingfei Lu, Yudi Qiu, Shiyan Yi, and Yibo Fan. A flexible embedding-aware near memory processing architecture for recommendation system. *IEEE Computer Architecture Letters*, 22(2):165–168, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LSJ⁺19] Chen Li, Yifan Sun, Lingling Jin, Lingjie Xu, Zheng Cao, Pengfei Fan, David Kaeli, Sheng Ma, Yang Guo, and Jun Yang. Priority-based PCIe scheduling for multi-tenant multi-GPU systems. *IEEE Computer Architecture*

- Letters*, 18(2):157–160, July 2019. ISSN 1556-6064.
- [Luo:2024:RMM] Haocong Luo, Yahya Can Tuğrul, F. Nisa Bostancı, Ataberk Olgun, A. Giray Yağlıkçı, and Onur Mutlu. Ramulator 2.0: a modern, modular, and extensible DRAM simulator. *IEEE Computer Architecture Letters*, 23(1):112–116, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LX08] Yun-Chen Lo, Yu-Chih Tsai, and Ren-Shuo Liu. LV: Latency-versatile floating-point engine for high-performance deep neural networks. *IEEE Computer Architecture Letters*, 22(2):125–128, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LTL23] Yun-Chen Lo, Yu-Chih Tsai, and Ren-Shuo Liu. LV: Latency-versatile floating-point engine for high-performance deep neural networks. *IEEE Computer Architecture Letters*, 22(2):125–128, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LWB13] Michael Lyons, Gu-Yeon Wei, and David Brooks. Shrink-Fit: a framework for flexible accelerator sizing. *IEEE Computer Architecture Letters*, 12(1):17–20, January/June 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Liu:2020:STA] Zhi-Gang Liu, Paul N. Whatmough, and Matthew Mattina. Systolic tensor array: an efficient structured-sparse GEMM accelerator for mobile CNN inference. *IEEE Computer Architecture Letters*, 19(1):34–37, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Lee:2008:PDD] J. Lee and X. Xiao. A parallel deadlock detection algorithm with $O(1)$ overall runtime complexity. *IEEE Computer Architecture Letters*, 7(2):45–48, July 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Liang:2016:CGR] Shuang Liang, Shouyi Yin, Leibo Liu, Yike Guo, and Shaojun Wei. A coarse-grained reconfigurable architecture for compute-intensive MapReduce acceleration. *IEEE Computer Architecture Letters*, 15(2):69–72, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Li:2020:DCA] Shang Li, Zhiyuan Yang, Dhiraaj Reddy, Ankur Srivastava, and Bruce Jacob. DRAMsim3: a cycle-accurate, thermal-capable DRAM simulator. *IEEE Computer Architecture Letters*, 19(2):106–109, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).

- [LYY⁺21] **Li:2021:HAG** Han Li, Mingyu Yan, Xiaocheng Yang, Lei Deng, Wenming Li, Xiaochun Ye, Dongrui Fan, and Yuan Xie. Hardware acceleration for GCNs via bidirectional fusion. *IEEE Computer Architecture Letters*, 20(1):66–4, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LZD⁺23] **Liu:2023:ILG** Jie Liu, Zhongyuan Zhao, Zijian Ding, Benjamin Brock, Hongbo Rong, and Zhiru Zhang. An intermediate language for general sparse format customization. *IEEE Computer Architecture Letters*, 22(2):153–156, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LZL⁺20] **Lee:2020:SFA** Joo Hwan Lee, Hui Zhang, Veronica Lagrange, Praveen Krishnamoorthy, Xiaodong Zhao, and Yang Seok Ki. SmartSSD: FPGA accelerated near-storage data analytics on SSD. *IEEE Computer Architecture Letters*, 19(2):110–113, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LZLX15] **Liao:2015:AWL** Jianwei Liao, Fengxiang Zhang, Li Li, and Guoqiang Xiao. Adaptive wear-leveling in flash-based memory. *IEEE Computer Architecture Letters*, 14(1):1–4, January/June 2015. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [LZS⁺08] **Li:2008:TAN** Z. Li, C. Zhu, L. Shang, R. Dick, and Y. Sun. Transaction-aware network-on-chip resource reservation. *IEEE Computer Architecture Letters*, 7(2):53–56, July 2008. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [MA19] **Marinakis:2019:PFI** Theodoros Marinakis and Iraklis Anagnostopoulos. Performance and fairness improvement on CMPs considering bandwidth and cache utilization. *IEEE Computer Architecture Letters*, 18(2):1–4, July 2019. ISSN 1556-6064.
- [MAHK18] **Min:2018:SCD** Seungwon Min, Mohammad Alian, Wen-Mei Hwu, and Nam Sung Kim. Semi-coherent DMA: an alternative I/O coherency management for embedded systems. *IEEE Computer Architecture Letters*, 17(2):221–224, July/December 2018. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).

- [Man15] Rajit Manohar. Comparing stochastic and deterministic computing. *IEEE Computer Architecture Letters*, 14(2):119–122, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [MCKW10] Ran Manevich, Israel Cidon, Avinoam Kolodny, and Isask'har Walter. Centralized adaptive routing for NoCs. *IEEE Computer Architecture Letters*, 9(2):57–60, July/December 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Mar13a] J. Martinez. A message from the new Editor-in-Chief and introduction of new Associate editors. *IEEE Computer Architecture Letters*, 12(1):2–4, January/June 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Mar13b] J. F. Martinez. Editorial. *IEEE Computer Architecture Letters*, 12(2):37–38, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [MAT17] Amirhossein Mirhosseini, Aditya Agrawal, and Josep Torrellas. Survive: Pointer-based in-DRAM incremental checkpointing for low-cost data persistence and rollback-recovery. *IEEE Computer Architecture Letters*, 16(2):153–157, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [MCM13] Rakan Maddah, Sangyeun Cho, and Rami Melhem. Data dependent sparing to manage better-than-bad blocks. *IEEE Computer Architecture Letters*, 12(2):43–46, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [MCRV07] M. Moreto Planas, F. Cazorla, A. Ramirez, and M. Valero. Explaining dynamic cache partitioning speed ups. *IEEE Computer Architecture Letters*, 6(1):1–4, January 2007. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [MCY⁺12] Justin Meza, Jichuan Chang, HanBin Yoon, Onur Mutlu, and Parthasarathy Ranganathan. Enabling efficient and scalable hybrid memories using fine-granularity DRAM cache management. *IEEE Computer Architecture*

Manohar:2015:CSD**Manevich:2010:CAR****Martinez:2013:MNE****Maddah:2013:DDS****Martinez:2013:E****MoretoPlanas:2007:EDC****Mirhosseini:2017:SPB****Meza:2012:EES**

- Letters*, 11(2):61–64, July/December 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [MGHP20]
- [MDK⁺23] **Moon:2023:AAD**
Yaebin Moon, Wanju Doh, Kwanhee Kyung, Eojin Lee, and Jung Ho Ahn. ADT: Aggressive demotion and promotion for tiered memory. *IEEE Computer Architecture Letters*, 22(1):21–24, January/June 2023. ISSN 1556-6056 (print), 1556-6064 (electronic). [MGI14]
- [MDSG20] **Mason:2020:UPI**
Tony Mason, Thaleia Dimitra Doudali, Margo Seltzer, and Ada Gavrilovska. Unexpected performance of Intel Optane DC persistent memory. *IEEE Computer Architecture Letters*, 19(1):55–58, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic). [MHAD15]
- [MGH⁺22] **Ma:2022:FBA**
Rui Ma, Evangelos Georganas, Alexander Heinecke, Sergey Gribok, Andrew Boutros, and Eriko Nurvitadhi. FPGA-Based AI smart NICs for scalable distributed AI training systems. *IEEE Computer Architecture Letters*, 21(2):49–52, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic). [MHM⁺24]
- Mirosanlou:2020:MED**
Reza Mirosanlou, Danlu Guo, Mohamed Hassan, and Rodolfo Pellizzoni. MCSim: an extensible DRAM memory controller simulator. *IEEE Computer Architecture Letters*, 19(2):105–109, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Martinsen:2014:HTL**
Jan Kasper Martinsen, Hakan Grahn, and Anders Isberg. Heuristics for thread-level speculation in Web applications. *IEEE Computer Architecture Letters*, 13(2):77–80, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Mohammadi:2015:DDB**
Milad Mohammadi, Song Han, Tor M. Aamodt, and William J. Dally. On-demand dynamic branch prediction. *IEEE Computer Architecture Letters*, 14(1):50–53, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Ma:2024:PFA**
Rui Ma, Jia-Ching Hsu, Ali Mansoorshahi, Joseph Garvey, Michael Kinsner, Deshanand Singh, and Derek Chiou. Primate: a framework to automatically generate soft

processors for network applications. *IEEE Computer Architecture Letters*, 23(1):57–60, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).

Michaud:2013:DMT

[Mic13]

Pierre Michaud. Demystifying multicore throughput metrics. *IEEE Computer Architecture Letters*, 12(2):63–66, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Michaud:2020:ETT

[Mic20]

Pierre Michaud. Exploiting thermal transients with deterministic turbo clock frequency. *IEEE Computer Architecture Letters*, 19(1):43–46, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).

Michelogiannakis:2011:PCE

[MJBD11]

George Michelogiannakis, Nan Jiang, Daniel U. Becker, and William J. Dally. Packet chaining: Efficient single-cycle allocation for on-chip networks. *IEEE Computer Architecture Letters*, 10(2):33–36, July/December 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Mars:2023:JPP

[MKD⁺23]

Jason Mars, Yiping Kang, Roland Daynauth, Baichuan

Li, Ashish Mahendra, Krisztian Flautner, and Lingjia Tang. The Jaseci programming paradigm and runtime stack: Building scale-out production applications easy and fast. *IEEE Computer Architecture Letters*, 22(2):101–104, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).

Marquez:2017:MCH

[MKM17]

David Gonzalez Marquez, Adrian Cristal Kestelman, and Esteban Mocskos. Mth: Codesigned hardware/software support for fine grain threads. *IEEE Computer Architecture Letters*, 16(1):64–67, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Mosquera:2023:GCC

[MKMJ23]

Fernando Mosquera, Krishna Kavi, Gayatri Mehta, and Lizy John. Guard cache: Creating noisy side-channels. *IEEE Computer Architecture Letters*, 22(2):97–100, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).

Mishra:2024:ASA

[MKP⁺24]

Deepanjali Mishra, Konstantinos Kanellopoulos, Ashish Panwar, Akshitha Sriraman, Vivek Seshadri, Onur Mutlu, and Todd C. Mowry. Address scaling: Architectural support for fine-grained thread-

- safe metadata management. *IEEE Computer Architecture Letters*, 23(1):69–72, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic). [MLK15]
- [MKSP05] O. Mutlu, Hyesoon Kim, J. Stark, and Y. N. Patt. On reusing the results of pre-executed instructions in a runahead execution processor. *IEEE Computer Architecture Letters*, 4(1):2, January 2005. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [MLM⁺06]
- [MLA⁺14] Hamid Mahmoodi, Sridevi Srinivasan Lakshmipuram, Manish Arora, Yashar Asgari, Houman Homayoun, Bill Lin, and Dean M. Tullsen. Resistive computation: a critique. *IEEE Computer Architecture Letters*, 13(2):89–92, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [MM03]
- [MLC24] Saurav Maji, Kyungmi Lee, and Anantha P. Chandrakasan. SparseLeakyNets: Classification prediction attack over sparsity-aware embedded neural networks using timing side-channel information. *IEEE Computer Architecture Letters*, 23(1):133–136, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic). [Manatunga:2015:HSS]
- Dilan Manatunga, Joo Hwan Lee, and Hyesoon Kim. Hardware support for safe execution of native client applications. *IEEE Computer Architecture Letters*, 14(1):37–40, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Mallik:2006:UDF]
- A. Mallik, B. Lin, G. Memik, P. Dinda, and R. P. Dick. User-driven frequency scaling. *IEEE Computer Architecture Letters*, 5(2):16, February 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Milenkovic:2003:SBT]
- A. Milenkovic and M. Milenkovic. Stream-based trace compression. *IEEE Computer Architecture Letters*, 2(1):4, January 2003. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Munoz-Martinez:2021:SEC]
- [MMAAK21] Francisco Muñoz-Martínez, José L. Abellán, Manuel E. Acacio, and Tushar Krishna. STONNE: Enabling cycle-level microarchitectural simulation for DNN inference accelerators. *IEEE Computer Architecture Letters*, 20(2):122–125, July/December

2021. ISSN 1556-6056 (print), 1556-6064 (electronic).

Martinez:2017:SII

[MMR17]

Jorge A. Martínez, Juan Antonio Maestro, and Pedro Reviriego. A scheme to improve the intrinsic error detection of the instruction set architecture. *IEEE Computer Architecture Letters*, 16(2):103–106, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Morad:2014:GMO

[MMY+14]

Amir Morad, Tomer Y. Morad, Leonid Yavits, Ran Ginosar, and Uri Weiser. Generalized MultiAmdahl: Optimization of heterogeneous multi-accelerator SoC. *IEEE Computer Architecture Letters*, 13(1):37–40, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Mikhailenko:2020:ASA

[MNFI20]

Darya Mikhailenko, Yujin Nakamoto, Ben Feinberg, and Engin Ipek. Adapting in situ accelerators for sparsity with granular matrix reordering. *IEEE Computer Architecture Letters*, 19(2):143–146, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).

[MNU+15]

Markovic:2015:TLS

Nikola Markovic, Daniel Nemirovsky, Osman Unsal, Mateo Valero, and Adrian Cristal. Thread lock section-aware scheduling on asymmetric single-ISA multi-core. *IEEE Computer Architecture Letters*, 14(2):160–163, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Min:2018:AAB

[MPA+18]

Donghyun Min, Donggyu Park, Jinwoo Ahn, Ryan Walker, Junghee Lee, Sungyong Park, and Youngjae Kim. Amoeba: an autonomous backup and recovery SSD for ransomware attack defense. *IEEE Computer Architecture Letters*, 17(2):243–246, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Manivannan:2017:RAG

[MPPS17]

Madhavan Manivannan, Miquel Pericàs, Vassilis Papaefstathiou, and Per Stenström. Runtime-assisted global cache management for task-based parallel programs. *IEEE Computer Architecture Letters*, 16(2):145–148, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Maycock:2016:HES

[MS16]

Matthew Maycock and Simha Sethumadhavan. Hardware

enforced statistical privacy. *IEEE Computer Architecture Letters*, 15(1):21–24, January/June 2016. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).

Matsuo:2019:IIF

[MSA19]

Reoma Matsuo, Ryota Shioya, and Hideki Ando. Improving the instruction fetch throughput with dynamically configuring the fetch pipeline. *IEEE Computer Architecture Letters*, 18(2):170–173, July 2019. ISSN 1556-6064.

Morad:2017:ORO

[MSE⁺17]

Tomer Y. Morad, Gil Shomron, Mattan Erez, Avinoam Kolodny, and Uri C. Weiser. Optimizing read-once data flow in big-data applications. *IEEE Computer Architecture Letters*, 16(1):68–71, January/June 2017. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).

Mashimo:2018:VMS

[MSI18]

Susumu Mashimo, Ryota Shioya, and Koji Inoue. VMOR: Microarchitectural support for operand access in an interpreter. *IEEE Computer Architecture Letters*, 17(2):217–220, July/December 2018. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).

Mars:2011:HHW

[MTH11]

Jason Mars, Lingjia Tang,

and Robert Hundt. Heterogeneity in “Homogeneous” warehouse-scale computers: a performance opportunity. *IEEE Computer Architecture Letters*, 10(2):29–32, July/December 2011. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).

Mouris:2018:TSB

[MTM18]

Dimitris Mouris, Nektarios Georgios Tsoutsos, and Michail Maniatakos. Terminator suite: Benchmarking privacy-preserving architectures. *IEEE Computer Architecture Letters*, 17(2):122–125, July/December 2018. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).

Miller:2012:MEP

[MTT12]

Timothy N. Miller, Renji Thomas, and Radu Teodorescu. Mitigating the effects of process variation in ultra-low voltage chip multiprocessors using dual supply voltages and half-speed units. *IEEE Computer Architecture Letters*, 11(2):45–48, July/December 2012. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).

Musoll:2009:PVA

[Mus09]

Enric Musoll. A process-variation aware technique for tile-based, massive multicore processors. *IEEE Computer*

- Architecture Letters*, 8(2):52–55, July/December 2009. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic). [MXS19]
- [MV15] Sparsh Mittal and Jeffrey S. Vetter. AYUSH: a technique for extending lifetime of SRAM–NVM hybrid caches. *IEEE Computer Architecture Letters*, 14(2):115–118, July/December 2015. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [MVJ17] Sparsh Mittal, Jeffrey S. Vetter, and Lei Jiang. Addressing read-disturbance issue in STT–RAM by data compression and selective duplication. *IEEE Computer Architecture Letters*, 16(2):94–98, July/December 2017. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [MWK⁺06] T. Y. Morad, U. C. Weiser, A. Kolodny, M. Valero, and E. Ayguade. Performance, power efficiency and scalability of asymmetric cluster chip multiprocessors. *IEEE Computer Architecture Letters*, 5(1):14–17, January 2006. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Mittal:2015:ATE] Mittal:2015:ATE
- [Mittal:2017:ARD] Mittal:2017:ARD
- [Morad:2006:PPE] Morad:2006:PPE
- [Masouros:2019:RRS] Masouros:2019:RRS
- D. Masouros, S. Xydis, and D. Soudris. Rusty: Runtime system predictability leveraging LSTM neural networks. *IEEE Computer Architecture Letters*, 18(2):103–106, July 2019. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Naghijouybari:2017:CCG] Naghibijouybari:2017:CCG
- Hoda Naghibijouybari and Nael Abu-Ghazaleh. Covert channels on GPGPUs. *IEEE Computer Architecture Letters*, 16(1):22–25, January/June 2017. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Nagabhiru:2024:AFP] Nagabhiru:2024:AFP
- [NB24] Mahita Nagabhiru and Gregory T. Byrd. Achieving forward progress guarantee in small hardware transactions. *IEEE Computer Architecture Letters*, 23(1):53–56, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Nilakantan:2013:MES] Nilakantan:2013:MES
- [NBH13] Siddharth Nilakantan, Steven Battle, and Mark Hempstead. Metrics for early-stage modeling of many-accelerator architectures. *IEEE Computer Architecture Letters*, 12(1):25–28, January/June 2013. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).

- Nam:2023:XRD**
- [NBW⁺23] Hwayong Nam, Seungmin Baek, Minbok Wi, Michael Jaemin Kim, Jaehyun Park, Chihun Song, Nam Sung Kim, and Jung Ho Ahn. X-ray: Discovering DRAM internal structure and error characteristics by issuing memory commands. *IEEE Computer Architecture Letters*, 22(2): 89–92, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic). [NK22]
- Naithani:2019:PRE**
- [NFAE19] Ajeya Naithani, Josue Feliu, Almutaz Adileh, and Lieven Eeckhout. Precise runahead execution. *IEEE Computer Architecture Letters*, 18(1): 71–74, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [NMS14]
- Nowatzki:2015:GBP**
- [NGS15] Tony Nowatzki, Venkatraman Govindaraju, and Karthikeyan Sankaralingam. A graph-based program representation for analyzing hardware specialization approaches. *IEEE Computer Architecture Letters*, 14(2):94–98, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [NPBS23]
- Nabavinejad:2019:CDP**
- [NHKR19] Seyed Morteza Nabavinejad, Hassan Hafez-Kolahi, and Sherief Reda. Coordinated DVFS and precision control for deep neural networks. *IEEE Computer Architecture Letters*, 18(2):136–140, July 2019. ISSN 1556-6064.
- Nye:2022:SSS**
- Jared Nye and Omer Khan. SSE: Security service engines to accelerate enclave performance in secure multi-core processors. *IEEE Computer Architecture Letters*, 21(2):129–132, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Nandakumar:2014:OKS**
- Vivek S. Nandakumar and Małgorzata Marek-Sadowska. On optimal kernel size for integrated CPU–GPUs — a case study. *IEEE Computer Architecture Letters*, 13(2): 81–84, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Nematallah:2023:ELS**
- Ahmed Nematallah, Chang Hyun Park, and David Black-Schaffer. Exploring the latency sensitivity of cache replacement policies. *IEEE Computer Architecture Letters*, 22(2):93–96, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).

- [NPS21] **Navarro:2021:HSS**
Marta Navarro, Lucia Pons, and Julio Sahuquillo. HySched: a simple hyperthreading-aware thread to core allocation strategy. *IEEE Computer Architecture Letters*, 20(1):26–29, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic). [NSF+18]
- [NR21] **Nabavinejad:2021:BLB**
Seyed Morteza Nabavinejad and Sherief Reda. BayesTuner: Leveraging Bayesian optimization for DNN inference configuration selection. *IEEE Computer Architecture Letters*, 20(2):166–170, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic). [ODKK18]
- [NS15] **Nathan:2015:AGC**
Ralph Nathan and Daniel J. Sorin. Argus-G: Comprehensive, low-cost error detection for GPGPU cores. *IEEE Computer Architecture Letters*, 14(1):13–16, January/June 2015. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [NSC20] **Newton:2020:PGP**
Newton, Virendra Singh, and Trevor E. Carlson. PIM-GraphSCC: PIM-based graph processing using graph’s community structures. *IEEE Computer Architecture Letters*, 19(2):151–154, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Nematollahi:2018:NSD**
Negin Nematollahi, Mohammad Sadrosadati, Hajar Falahati, Marzieh Barkhordar, and Hamid Sarbazi-Azad. Neda: Supporting direct inter-core neighbor data exchange in GPUs. *IEEE Computer Architecture Letters*, 17(2):225–229, July/December 2018. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Omar:2018:MRI**
Hamza Omar, Halit Dogan, Brian Kahne, and Omer Khan. Multicore resource isolation for deterministic, resilient and secure concurrent execution of safety-critical applications. *IEEE Computer Architecture Letters*, 17(2):230–234, July/December 2018. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Omori:2022:OSH**
Yu Omori and Keiji Kimura. Open-source hardware memory protection engine integrated with NVMM simulator. *IEEE Computer Architecture Letters*, 21(2):77–80, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).

- [OKS⁺15] **O:2015:CCI**
 Seongil O, Sanghyuk Kwon, Young Hoon Son, Yujin Park, and Jung Ho Ahn. CIDR: a cache inspired area-efficient DRAM resilience architecture against permanent faults. *IEEE Computer Architecture Letters*, 14(1):17–20, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [ORS⁺06] **Ottoni:2006:SPC**
 G. Ottoni, R. Rangan, A. Stoler, M. J. Bridges, and D. I. August. From sequential programs to concurrent threads. *IEEE Computer Architecture Letters*, 5(1):6–9, January 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [OSH16] **Olson:2016:SIT**
 Lena E. Olson, Simha Sethumadhavan, and Mark D. Hill. Security implications of third-party accelerators. *IEEE Computer Architecture Letters*, 15(1):50–53, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [PB16] **Panda:2016:EPP**
 Biswabandan Panda and Shankar Balachandran. Expert prefetch prediction: an expert predicting the usefulness of hardware prefetchers. *IEEE Computer Architecture Letters*, 15(1):13–16, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [PBO⁺15] **Pekhimenko:2015:TAC**
 Gennady Pekhimenko, Evgeny Bolotin, Mike O’Connor, Onur Mutlu, Todd C. Mowry, and Stephen W. Keckler. Toggle-aware compression for GPUs. *IEEE Computer Architecture Letters*, 14(2):164–168, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [PDGV16] **Pu:2016:NIP**
 Libei Pu, Kshitij Doshi, Ellis Giles, and Peter Varman. Non-intrusive persistence with a backend NVM controller. *IEEE Computer Architecture Letters*, 15(1):29–32, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Per21] **Perais:2021:CSS**
 Arthur Perais. A case for speculative strength reduction. *IEEE Computer Architecture Letters*, 20(1):22–25, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [PGC22] **Piccolboni:2022:ASS**
 Luca Piccolboni, Davide Giri, and Luca P. Carloni. Accelerators & security: The socket approach. *IEEE Computer*

- Architecture Letters*, 21(2): 65–68, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic). [PHO⁺15]
- [PGJ12] **Panda:2012:BFB**
Reena Panda, Paul V. Gratz, and Daniel A. Jiménez. B-Fetch: Branch prediction directed prefetching for in-order processors. *IEEE Computer Architecture Letters*, 11(2): 41–44, July/December 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [PJ22]
- [PGR⁺23] **Patel:2023:TIP**
Pratyush Patel, Zibo Gong, Syeda Rizvi, Esha Choukse, Pulkit Misra, Thomas Anderson, and Akshitha Sri-raman. Towards improved power management in cloud GPUs. *IEEE Computer Architecture Letters*, 22(2):141–144, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic). [PKKK23]
- [PHBC18] **Pham:2018:TSM**
Binh Pham, Derek Hower, Abhishek Bhattacharjee, and Trey Cain. TLB shoot-down mitigation for low-power many-core servers with L1 virtual caches. *IEEE Computer Architecture Letters*, 17(1):17–20, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [PL10]
- Power:2015:GGH**
Jason Power, Joel Hestness, Marc S. Orr, Mark D. Hill, and David A. Wood. gem5-gpu: a heterogeneous CPU–GPU simulator. *IEEE Computer Architecture Letters*, 14(1):34–36, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Park:2022:SML**
Jongwon Park and Jinkyu Jeong. Speculative multi-level access in LSM tree-based KV store. *IEEE Computer Architecture Letters*, 21(2):145–148, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Park:2023:CEE**
Gyeongseo Park, Ki-Dong Kang, Minho Kim, and Daehoon Kim. CoreNap: Energy efficient core allocation for latency-critical workloads. *IEEE Computer Architecture Letters*, 22(1):1–4, January/June 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Patil:2010:URT**
Shruti Patil and David J. Lilja. Using resampling techniques to compute confidence intervals for the harmonic mean of rate-based performance metrics. *IEEE Computer Architecture Letters*, 9

(1):1–4, January/June 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Poluri:2015:SET

[PL15]

Pavan Poluri and Ahmed Louri. A soft error tolerant network-on-chip router pipeline for multi-core systems. *IEEE Computer Architecture Letters*, 14(2):107–110, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Park:2023:DHP

[PLK⁺23]

Chanyoung Park, Chun-Yi Liu, Kyungtae Kang, Mahmut Kandemir, and Wonil Choi. Design of a high-performance, high-endurance key-value SSD for large-key workloads. *IEEE Computer Architecture Letters*, 22(2):149–152, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).

Pao:2008:PAM

[PLL08]

D. Pao, W. Lin, and B. Liu. Pipelined architecture for multi-string matching. *IEEE Computer Architecture Letters*, 7(2):33–36, July 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Piscitelli:2012:HLP

[PP12]

Roberta Piscitelli and Andy D. Pimentel. A high-level power

model for MPSoC on FPGA. *IEEE Computer Architecture Letters*, 11(1):13–16, January/June 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Park:2024:DND

[PPA⁺24]

Yongmo Park, Subhankar Pal, Aporva Amarnath, Karthik Swaminathan, Wei D. Lu, Alper Buyuktosunoglu, and Pradip Bose. Dramaton: a near-DRAM accelerator for large number theoretic transforms. *IEEE Computer Architecture Letters*, 23(1):108–111, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).

Prieto:2011:MCM

[PPG11]

Pablo Prieto, Valentin Puente, and Jose-Angel Gregorio. Multilevel cache modeling for chip-multiprocessor systems. *IEEE Computer Architecture Letters*, 10(2):49–52, July/December 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Pinto:2017:TTA

[PPG⁺17]

Sandro Pinto, Jorge Pereira, Tiago Gomes, Mongkol Ekpanyapong, and Adriano Tavares. Towards a TrustZone-assisted hypervisor for real-time embedded systems. *IEEE Computer Architecture Letters*, 16(2):158–161, July/December 2017. CODEN ????

ISSN 1556-6056 (print), 1556-6064 (electronic).

Perais:2017:SFM

[PS17]

Arthur Perais and Andre Sez nec. Storage-free memory dependency prediction. *IEEE Computer Architecture Letters*, 16(2):149–152, July/December 2017. CODEN ????? [QYZ+24] ISSN 1556-6056 (print), 1556-6064 (electronic).

Peltekis:2024:DDM

[PTND24]

Christodoulos Peltekis, Vasileios Titopoulos, Chrysostomos Nicopoulos, and Giorgos Dimitrakopoulos. DeMM: a decoupled matrix multiplication engine supporting relaxed structured sparsity. *IEEE Computer Architecture Letters*, 23(1):17–20, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic). [RAD+23]

Price:2006:CCT

[PV06]

G. Price and M. Vachharajani. A case for compressing traces with BDDs. *IEEE Computer Architecture Letters*, 5(2):18, February 2006. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).

Poremba:2015:NUF

[PZX15]

Matthew Poremba, Tao Zhang, and Yuan Xie. NVMain 2.0: a user-friendly memory simulator to model

(non-) volatile memory systems. *IEEE Computer Architecture Letters*, 14(2):140–143, July/December 2015. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).

Qi:2024:AIG

Yingjie Qi, Jianlei Yang, Ao Zhou, Tong Qiao, and Chunming Hu. Architectural implications of GNN aggregation programming abstractions. *IEEE Computer Architecture Letters*, 23(1):125–128, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).

Ringlein:2023:ACD

Burkhard Ringlein, Francois Abel, Dionysios Diamantopoulos, Beat Weiss, Christoph Hagleitner, and Dietmar Fey. Advancing compilation of DNNs for FPGAs using operation set architectures. *IEEE Computer Architecture Letters*, 22(1):9–12, January/June 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).

Rao:2019:ATC

[RADZ19]

J. Rao, T. Ao, K. Dai, and X. Zou. ARCE: Towards code pointer integrity on embedded processors using architecture-assisted run-time metadata management. *IEEE Computer Architecture Letters*, 18(2):115–118, July 2019. ISSN

1556-6056 (print), 1556-6064 (electronic).

Ranganath:2019:SCC

- [RASW19] Kiran Ranganath, AmirAli Abdolrashidi, Shuaiwen Leon Song, and Daniel Wong. Speeding up collective communications through inter-GPU re-routing. *IEEE Computer Architecture Letters*, 18(2):128–131, July 2019. ISSN 1556-6064.

Rotem:2014:BUI

- [RB14] Nadav Rotem and Yosi Ben Asher. Block unification IF-conversion for high performance architectures. *IEEE Computer Architecture Letters*, 13(1):17–20, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Rosenfeld:2011:DCA

- [RCBJ11] Paul Rosenfeld, Elliott Cooper-Balis, and Bruce Jacob. DRAMSim2: a cycle accurate memory system simulator. *IEEE Computer Architecture Letters*, 10(1):16–19, January/June 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Resch:2021:CPC

- [RCK21] Salonik Resch, Husrev Cilason, and Ulya R. Karpuzcu. Cryogenic PIM: Challenges opportunities. *IEEE Computer Architecture Letters*, 20(1):74–77, January/June

2021. ISSN 1556-6056 (print), 1556-6064 (electronic).

Rodopoulos:2015:TPV

- [RCS15] Dimitrios Rodopoulos, Francky Catthoor, and Dimitrios Soudris. Tackling performance variability due to RAS mechanisms with PID-controlled DVFS. *IEEE Computer Architecture Letters*, 14(2):156–159, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Ros:2020:EIP

- [RJ20] Alberto Ros and Alexandra Jimborean. The entangling instruction prefetcher. *IEEE Computer Architecture Letters*, 19(2):84–87, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).

Resch:2022:VSQ

- [RK22] Salonik Resch and Ulya Karpuzcu. On variable strength quantum ECC. *IEEE Computer Architecture Letters*, 21(2):93–96, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).

Ramanujam:2008:RPM

- [RL08] R. Sunkam Ramanujam and B. Lin. Randomized partially-minimal routing on three-dimensional mesh networks. *IEEE Computer Architecture Letters*, 7(2):37–40, July

2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Ramanujam:2009:WRR

[RL09]

Rohit Sunkam Ramanujam and Bill Lin. Weighted random routing on torus networks. *IEEE Computer Architecture Letters*, 8(1):1–4, January/June 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Ravi:2017:TSM

[RL17]

Gokul Subramanian Ravi and Mikko Lipasti. Timing speculation in multi-cycle data paths. *IEEE Computer Architecture Letters*, 16(1):84–87, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Rakshit:2018:LLO

[RM18]

Joydeep Rakshit and Kartik Mohanram. LEO: Low overhead encryption ORAM for non-volatile memories. *IEEE Computer Architecture Letters*, 17(2):100–104, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Rezaei:2020:NNM

[RMA⁺20]

Seyyed Hossein SeyyedAghaei Rezaei, Mehdi Modarressi, Rachata Ausavarungnirun, Mohammad Sadrosadati, Onur Mutlu, and Masoud Danesh-talab. NoM: Network-on-memory for inter-bank data

transfer in highly-banked memories. *IEEE Computer Architecture Letters*, 19(1):80–83, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).

Rezaei:2024:SMD

[RMM24]

Seyyed Hossein SeyyedAghaei Rezaei, Parham Zilouchian Moghaddam, and Mehdi Modarressi. Smart memory: Deep learning acceleration in 3D-stacked memories. *IEEE Computer Architecture Letters*, 23(1):137–141, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).

Rezaei:2016:DRS

[RMMLK16]

Seyyed Hossein Seyyedaghaei Rezaei, Abbas Mazloumi, Mehdi Modarressi, and Pejman Lotfi-Kamran. Dynamic resource sharing for high-performance 3-D networks-on-chip. *IEEE Computer Architecture Letters*, 15(1):5–8, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Roth:2008:PRR

[Rot08]

A. Roth. Physical register reference counting. *IEEE Computer Architecture Letters*, 7(1):9–12, January 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [RSO21] **Rucker:2021:CTB**
Alexander Rucker, Muhammad Shahbaz, and Kunle Olukotun. Chopping off the tail: Bounded non-determinism for real-time accelerators. *IEEE Computer Architecture Letters*, 20(2):110–113, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [RSRT19] **Rogers:2019:SLB**
Samuel Rogers, Joshua Slycord, Ronak Raheja, and Hamed Tabkhi. Scalable LLVM-based accelerator modeling in gem5. *IEEE Computer Architecture Letters*, 18(1):18–21, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [RTKQ21] **Resch:2021:DLQ**
Salonik Resch, Swamit Tannu, Ulya R. Karpuzcu, and Moinuddin Qureshi. A day in the life of a quantum error. *IEEE Computer Architecture Letters*, 20(1):13–16, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [RYSN04] **Robotmili:2004:TSI**
B. Robotmili, N. Yazdani, S. Sardashti, and M. Nourani. Thread-sensitive instruction issue for SMT processors. *IEEE Computer Architecture Letters*, 3(1):5, January 2004. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [RZ06] **Riley:2006:PCU**
N. Riley and C. Zilles. Probabilistic counter updates for predictor hysteresis and bias. *IEEE Computer Architecture Letters*, 5(1):18–21, January 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SAA+23] **Sim:2023:CCM**
Joonseop Sim, Soohong Ahn, Taeyoung Ahn, Seungyong Lee, Myunghyun Rhee, Jooyoung Kim, Kwangsik Shin, Donguk Moon, Euseok Kim, and Kyoung Park. Computational CXL-Memory solution for accelerating memory-intensive applications. *IEEE Computer Architecture Letters*, 22(1):5–8, January/June 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SB18] **Shwartz:2018:DMI**
Ofir Shwartz and Yitzhak Birk. Distributed memory integrity trees. *IEEE Computer Architecture Letters*, 17(2):159–162, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SBQK21] **Shoghi:2021:SSQ**
Nima Shoghi, Andrei Bersatti, Moinuddin Qureshi, and Hye-soon Kim. SmaQ: Smart

- quantization for DNN training by exploiting value clustering. *IEEE Computer Architecture Letters*, 20(2):126–129, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic). [SCL06]
- [SBVB17] **Sasaki:2017:MPC**
Hiroshi Sasaki, Alper Buyuktosunoglu, Augusto Vega, and Pradip Bose. Mitigating power contention: a scheduling based approach. *IEEE Computer Architecture Letters*, 16(1):60–63, January/June 2017. CODEN ??? ISSN 1556-6056 (print), 1556-6064 (electronic). [SCL13]
- [SCB+20] **Sutradhar:2020:PPP**
Purab Ranjan Sutradhar, Mark Connolly, Sathwika Bavikadi, Sai Manoj Pudukotai Dinakarrao, Mark A. Indovina, and Amlan Ganguly. pPIM: a programmable processor-in-memory architecture with precision-scaling for deep learning. *IEEE Computer Architecture Letters*, 19(2):118–121, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic). [SCR+17]
- [SCF04] **Stine:2004:CAR**
J. M. Stine, N. P. Carter, and J. Flich. Comparing adaptive routing and dynamic voltage scaling for link power reduction. *IEEE Computer Architecture Letters*, 3(1):4, January 2004. CODEN ??? ISSN 1556-6056 (print), 1556-6064 (electronic). [SD02]
- Srinivasan:2006:PMU**
R. Srinivasan, J. Cook, and O. Lubeck. Performance modeling using Monte Carlo simulation. *IEEE Computer Architecture Letters*, 5(1):38–41, January 2006. CODEN ??? ISSN 1556-6056 (print), 1556-6064 (electronic). [Sun:2013:NWC]
- Guang Sun, Chia-Wei Chang, and Bill Lin. A new worst-case throughput bound for oblivious routing in odd radix mesh network. *IEEE Computer Architecture Letters*, 12(1):9–12, January/June 2013. CODEN ??? ISSN 1556-6056 (print), 1556-6064 (electronic). [Son:2017:SAS]
- Young Hoon Son, Hyunyoong Cho, Yuhwan Ro, Jae W. Lee, and Jung Ho Ahn. SALAD: Achieving symmetric access latency with asymmetric DRAM architecture. *IEEE Computer Architecture Letters*, 16(1):76–79, January/June 2017. CODEN ??? ISSN 1556-6056 (print), 1556-6064 (electronic). [Shaw:2002:MSC]
- K. A. Shaw and W. J. Dally. Migration in single chip multiprocessors. *IEEE Computer Architecture Letters*, 1(1):12,

- January 2002. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SD04] **Singh:2004:BDB** [SFFG⁺19] A. Singh and W. J. Dally. Buffer and delay bounds in high radix interconnection networks. *IEEE Computer Architecture Letters*, 3(1):8, January 2004. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SDTG04] **Singh:2004:GAL** [SG14] A. Singh, W. J. Dally, B. Towles, and A. K. Gupta. Globally adaptive load-balanced routing on tori. *IEEE Computer Architecture Letters*, 3(1):2, January 2004. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Sez10] **Seznec:2010:PCM** [SGBE18] Andre Seznec. A phase change memory as a secure main memory. *IEEE Computer Architecture Letters*, 9(1):5–8, January/June 2010. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SfCL03] **Sendag:2003:ACE** [SHB⁺15] R. Sendag, Peng fei Chuang, and D. J. Lilja. Address correlation: Exceeding the limits of locality. *IEEE Computer Architecture Letters*, 2(1):3, January 2003. CODEN
- ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Stow:2019:PPM** Dylan Stow, Amin Farmahini-Farahani, Sudhanva Gurusururthi, Michael Ignatowski, and Yuan Xie. Power profiling of modern die-stacked memory. *IEEE Computer Architecture Letters*, 18(2):132–135, July 2019. ISSN 1556-6064.
- Sankar:2014:SFL** Sriram Sankar and Sudhanva Gurusururthi. Soft failures in large datacenters. *IEEE Computer Architecture Letters*, 13(2):105–108, July/December 2014. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic).
- SanMiguel:2018:EMA** Joshua San Miguel, Karthik Ganesan, Mario Badr, and Natalie Enright Jerger. The EH model: Analytical exploration of energy-harvesting architectures. *IEEE Computer Architecture Letters*, 17(1):76–79, January/June 2018. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic).
- Seshadri:2015:FBB** Vivek Seshadri, Kevin Hsieh, Amirali Boroum, Donghyuk Lee, Michael A. Kozuch, Onur Mutlu, Phillip B. Gibbons, and Todd C. Mowry. Fast

- bulk bitwise AND and OR in DRAM. *IEEE Computer Architecture Letters*, 14(2):127–131, July/December 2015. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic). [SJ22]
- [SHJW21] Jiya Su, Linfeng He, Peng Jiang, and Rujia Wang. Exploring PIM architecture for high-performance graph pattern mining. *IEEE Computer Architecture Letters*, 20(2):114–117, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SHK15] Qingchuan Shi, Henry Hoffmann, and Omer Khan. A cross-layer multicore architecture to tradeoff program accuracy and resilience overheads. *IEEE Computer Architecture Letters*, 14(2):85–89, July/December 2015. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SHW19] G. Shomron, T. Horowitz, and U. Weiser. SMT-SA: Simultaneous multithreading in systolic arrays. *IEEE Computer Architecture Letters*, 18(2):99–102, July 2019. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SJA⁺17] Wonjun Song, Hyung-Joon Jung, Jung Ho Ahn, Jae W. Lee, and John Kim. Evaluation of performance unfairness in NUMA system architecture. *IEEE Computer Architecture Letters*, 16(1):26–29, January/June 2017. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SJM02] YoungChul Sohn, NaiHoon Jung, and Seungryoul Maeng. Request reordering to enhance the performance of strict consistency models. *IEEE Computer Architecture Letters*, 1(1):11, January 2002. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SJM17] Seyed Mohammad Seyedzadeh, Alex K. Jones, and Rami Melhem. Counter-based tree structure for row hammering mitigation in DRAM. *IEEE Computer Architecture Letters*, 16(1):18–21, January/
- Salvesen:2022:LAR**
- Peter Salvesen and Magnus Jahre. LMT: Accurate and resource-scalable slowdown prediction. *IEEE Computer Architecture Letters*, 21(2):97–100, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Su:2021:EPA**
- Song:2017:EPU**
- Shi:2015:CLM**
- Sohn:2002:RRE**
- Shomron:2019:SSS**
- Seyedzadeh:2017:CBT**

- June 2017. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic). [Ska10a]
- [SJS24] Mrinmay Sasmal, Tresa Joseph, and Bindiya T. S. Approximate multiplier design with LFSR-based stochastic sequence generators for edge AI. *IEEE Computer Architecture Letters*, 23(1):91–94, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SK21] Mohsin Shan and Omer Khan. Accelerating concurrent priority scheduling using adaptive in-hardware task distribution in multi-cores. *IEEE Computer Architecture Letters*, 20(1):17–21, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ska09a] K. Skadron. Letter from the Editor. *IEEE Computer Architecture Letters*, 8(2):39, July/December 2009. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ska09b] Kevin Skadron. Untitled. *IEEE Computer Architecture Letters*, 8(2):39, July/December 2009. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ska10a] K. Skadron. Editorial: Letter from the Editor-in-Chief. *IEEE Computer Architecture Letters*, 9(2):37–44, July/December 2010. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ska10b] Kevin Skadron. Untitled. *IEEE Computer Architecture Letters*, 9(2):37–44, July/December 2010. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ska11a] K. Skadron. Editorial: Letter from the Editor-in-Chief. *IEEE Computer Architecture Letters*, 10(1):1–3, January/June 2011. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ska11b] Kevin Skadron. Untitled. *IEEE Computer Architecture Letters*, 10(1):1–3, January/June 2011. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Ska13] Kevin Skadron. Introducing the new Editor-in-Chief of the *IEEE Computer Architecture Letters*. *IEEE Computer Architecture Letters*, 12(1):1, January/June 2013. CODEN ????
- ISSN 1556-6056 (print), 1556-6064 (electronic).

- [SKA⁺20] **Sartor:2020:HHL**
Anderson L. Sartor, Anish Krishnakumar, Samet E. Arda, Umit Y. Ogras, and Radu Marculescu. HiLITE: Hierarchical and lightweight imitation learning for power management of embedded SoCs. *IEEE Computer Architecture Letters*, 19(1):63–67, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SKD09] **Sudarsanam:2009:PPD**
Arvind Sudarsanam, Ramachandra Kallam, and Aravind Dasu. PRR–PRR dynamic relocation. *IEEE Computer Architecture Letters*, 8(2):44–47, July/December 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SKK22] **Shin:2022:OOS**
Gyeongcheol Shin, Junsoo Kim, and Joo-Young Kim. OpenMDS: an open-source shell generation framework for high-performance design on Xilinx multi-die FPGAs. *IEEE Computer Architecture Letters*, 21(2):101–104, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SKS⁺15] **Seongil:2015:CCI**
O. Seongil, Sanghyuk Kwon, Young Hoon Son, Yujin Park, and Jung Ho Ahn. CIDR: a cache inspired area-efficient DRAM resilience architecture against permanent faults. *IEEE Computer Architecture Letters*, 14(1):17–20, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SKS⁺24] **Shin:2024:CMR**
Changmin Shin, Taehee Kwon, Jaeyong Song, Jae Hyung Ju, Frank Liu, Yeonkyu Choi, and Jinho Lee. A case for in-memory random scatter-gather for fast graph processing. *IEEE Computer Architecture Letters*, 23(1):73–77, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SKTC05] **Sazeides:2005:DIB**
Y. Sazeides, R. Kumar, D. M. Tullsen, and T. Constantinou. The danger of interval-based power efficiency metrics: When worst is best. *IEEE Computer Architecture Letters*, 4(1):1, January 2005. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SLC03] **Sihn:2003:SCS**
K.-H. Sihn, Joonwon Lee, and Jung-Wan Cho. A speculative coherence scheme using decoupling synchronization for multiprocessor systems. *IEEE Computer Architecture Letters*, 2(1):1, January 2003. CODEN ????.

- ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SLKD14] Keun Sup Shim, Mieszko Lis, Omer Khan, and Srinivas Devadas. Thread migration prediction for distributed shared caches. *IEEE Computer Architecture Letters*, 13(1):53–56, January/June 2014. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SMZ18] **Shim:2014:TMP** Alberto Scionti, Somnath Mazumdar, and Stephane Zuckerman. Enabling massive multi-threading with fast hashing. *IEEE Computer Architecture Letters*, 17(1):1–4, January/June 2018. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SM18] **Swami:2018:AAS** Shivam Swami and Kartik Mohanram. ARSENAL: Architecture for secure non-volatile memories. *IEEE Computer Architecture Letters*, 17(2):192–196, July/December 2018. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SPAP10] **Subramoni:2010:ISI** Hari Subramoni, Fabrizio Petrini, Virat Agarwal, and Davide Pasetto. Intra-socket and inter-socket communication in multi-core systems. *IEEE Computer Architecture Letters*, 9(1):13–16, January/June 2010. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SMLS15] **Seo:2015:DDF** Bon-Keun Seo, Seungryoul Maeng, Joonwon Lee, and Euseong Seo. DRACO: a deduplicating FTL for tangible extra capacity. *IEEE Computer Architecture Letters*, 14(2):123–126, July/December 2015. CODEN ????. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SPHS22] **Shin:2022:RSA** Yongwon Shin, Juseong Park, Jeongmin Hong, and Hyojin Sung. Runtime support for accelerating CNN models on digital DRAM processing-in-memory hardware. *IEEE Computer Architecture Letters*, 21(2):33–36, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SMY15] **Song:2015:ARL** William Song, Saibal Mukhopadhyay, and Sudhakar Yalamanchili. Architectural reliability: Lifetime reliability

- [SPJ02] **Shang:2002:PEI**
Li Shang, L. Peh, and N. K. Jha. Power-efficient interconnection networks: Dynamic voltage scaling with links. *IEEE Computer Architecture Letters*, 1(1):6, January 2002. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SQ23] **Saileshwar:2023:MBM**
Gururaj Saileshwar and Moinuddin Qureshi. The mirage of breaking MIRAGE: Analyzing the modeling pitfalls in emerging attacks on MIRAGE. *IEEE Computer Architecture Letters*, 22(2):121–124, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SRH20] **Sharifi:2020:AAC**
Ferdous Sharifi, Nezam Rohbani, and Shaahin Hessabi. Aging-aware context switching in multicore processors based on workload classification. *IEEE Computer Architecture Letters*, 19(2):159–162, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SRLM20] **Singh:2020:VLB**
Rahul Singh, Gokul Subramanian Ravi, Mikko Lipasti, and Joshua San Miguel. Value locality based approximation with ODIN. *IEEE Computer Architecture Letters*, 19(2):88–91, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SRLP09] **Soteriou:2009:HTD**
Vassos Soteriou, Rohit Sunkam Ramanujam, Bill Lin, and Li-Shiuan Peh. A high-throughput distributed shared-buffer NoC router. *IEEE Computer Architecture Letters*, 8(1):21–24, January/June 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SRS11] **Siozios:2011:SRT**
Kostas Siozios, Dimitrios Rodopoulos, and Dimitrios Soudris. On supporting rapid thermal analysis. *IEEE Computer Architecture Letters*, 10(2):53–56, July/December 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SRS20] **Sadredini:2020:ESP**
Elaheh Sadredini, Reza Rahimi, and Kevin Skadron. Enabling in-SRAM pattern processing with low-overhead reporting architecture. *IEEE Computer Architecture Letters*, 19(2):167–170, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SRT12] **Sethumadhavan:2012:CHD**
Simha Sethumadhavan, Ryan Roberts, and Yannis Tsiavidis. A case for hybrid

- discrete-continuous architectures. *IEEE Computer Architecture Letters*, 11(1):1–4, January/June 2012. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic). [SSTS17]
- [SRV⁺19] E. Sadredini, R. Rahimi, V. Verma, M. Stan, and K. Skadron. A scalable and efficient in-memory interconnect architecture for automata processing. *IEEE Computer Architecture Letters*, 18(2):87–90, July 2019. ISSN 1556-6056 (print), 1556-6064 (electronic). **Sadredini:2019:SEM**
- [SSS⁺21] Parth Shah, Ranjal Gautham Shenoy, Vaidyanathan Srinivasan, Pradip Bose, and Alper Buyuktosunoglu. TokenSmart: Distributed, scalable power management in the many-core era. *IEEE Computer Architecture Letters*, 20(1):42–45, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic). **Shah:2021:TDS**
- [SSSM18] Debiprasanna Sahoo, Swaraj Sha, Manoranjan Satpathy, and Madhu Mutyam. ReDRAM: a reconfigurable DRAM cache for GPGPUs. *IEEE Computer Architecture Letters*, 17(2):213–216, July/December 2018. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic). **Sahoo:2018:RRD**
- [ST20] Ahmed Samara and James Tuck. The case for domain-specialized branch predictors for graph-processing. *IEEE Computer Architecture Letters*, 19(2):101–104, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic). **Samara:2020:CDS**
- [SW16] Rathijit Sen and David A. Wood. GPGPU footprint models to estimate per-core power. *IEEE Computer Architecture Letters*, 16(1):34–37, January/June 2017. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic). **Sen:2016:GFM**
- [SSVS21] Arindam Sarkar, Newton Singh, Varun Venkitaraman, and Virendra Singh. DAM: Deadblock aware migration techniques for STT-RAM-based hybrid caches. *IEEE Computer Architecture Letters*, 20(1):62–4, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic). **Sarkar:2021:DDA**
- [Sasaki:2017:HTP] Hiroshi Sasaki, Fang-Hsiang Su, Teruo Tanimoto, and Simha Sethumadhavan. Heavy tails in program structure. *IEEE Computer Architecture Letters*, 16(1):34–37, January/June 2017. CODEN ????? ISSN 1556-6056 (print), 1556-6064 (electronic). **Sasaki:2017:HTP**

- Architecture Letters*, 15(2): 97–100, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [SW19] **Shomron:2019:SCV**
Gil Shomron and Uri Weiser. Spatial correlation and value prediction in convolutional neural networks. *IEEE Computer Architecture Letters*, 18(1):10–13, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [TD02]
- [SYC07] **Sendag:2007:BMP**
R. Sendag, J. Yi, and P. Chuang. Branch misprediction prediction: Complementary branch predictors. *IEEE Computer Architecture Letters*, 6(2):49–52, February 2007. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [TDO16]
- [SYC14] **Song:2014:AFB**
Xiang Song, Jian Yang, and Haibo Chen. Architecting flash-based solid-state drive for high-performance I/O virtualization. *IEEE Computer Architecture Letters*, 13(2): 61–64, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [TLG⁺11]
- [TASA13] **Tavakkol:2013:NSS**
Arash Tavakkol, Mohammad Arjomand, and Hamid Sarbazi-Azad. Network-on-SSD: a scalable and high-performance communication design paradigm for SSDs. *IEEE Computer Architecture Letters*, 12(1):5–8, January/June 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Towles:2002:WCT]
- B. Towles and W. J. Dally. Worst-case traffic for oblivious routing functions. *IEEE Computer Architecture Letters*, 1(1):4, January 2002. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Tomusk:2016:DDG]
- Erik Tomusk, Christophe Dubach, and Michael O’Boyle. Diversity: a design goal for heterogeneous processors. *IEEE Computer Architecture Letters*, 15(2):81–84, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Tang:2011:PEM]
- Jie Tang, Shaoshan Liu, Zhimin Gu, Chen Liu, and Jean-Luc Gaudiot. Prefetching in embedded mobile systems can be energy-efficient. *IEEE Computer Architecture Letters*, 10(1):8–11, January/June 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [TMNK19] **Tovletoglou:2019:SIH**
Konstantinos Tovletoglou, Lev Mukhanov, Dimitrios S. Nikolopoulos, and Georgios Karakonstantis. Shimmer: Implementing a heterogeneous-reliability DRAM framework on a commodity server. *IEEE Computer Architecture Letters*, 18(1):26–29, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [TMSA16] **Tavakkol:2016:TTB**
Arash Tavakkol, Pooyan Mehrvarzy, and Hamid Sarbazi-Azad. TBM: Twin block management policy to enhance the utilization of plane-level parallelism in SSDs. *IEEE Computer Architecture Letters*, 15(2):121–124, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [TMSX23] **Tzenetopoulos:2023:DLD**
Achilleas Tzenetopoulos, Dimosthenis Masouros, Dimitrios Soudris, and Sotirios Xydis. DVFaaS: Leveraging DVFS for FaaS workflows. *IEEE Computer Architecture Letters*, 22(2):85–88, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [TNC19] **Tan:2019:DWO**
Tian Tan, Eriko Nurvitadhi, and Derek Chiou. Dark wires and the opportunities for reconfigurable logic. *IEEE Computer Architecture Letters*, 18(1):67–70, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [TND⁺21] **Tan:2021:FQF**
Tian Tan, Eriko Nurvitadhi, Aravind Dasu, Martin Langhammer, and Derek Chiou. FlexScore: Quantifying flexibility. *IEEE Computer Architecture Letters*, 20(1):58–4, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [TOIS17] **Tanimoto:2017:EDG**
Teruo Tanimoto, Takatsugu Ono, Koji Inoue, and Hiroshi Sasaki. Enhanced dependence graph model for critical path analysis on modern out-of-order processors. *IEEE Computer Architecture Letters*, 16(2):111–114, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [TS24] **Tsantikidou:2024:AEA**
Kyriaki Tsantikidou and Nicolas Sklavos. An area efficient architecture of a novel chaotic system for high randomness security in e-health. *IEEE Computer Architecture Letters*, 23(1):104–107, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).

- [TV02] **Tambat:2002:PLB**
S. Tambat and S. Vajapeyam. Page-level behavior of cache contention. *IEEE Computer Architecture Letters*, 1(1):9, January 2002. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [TVB⁺13] **Tembey:2013:SSS**
Priyanka Tembey, Augusto Vega, Alper Buyuktosunoglu, Dilma Da Silva, and Pradip Bose. SMT switch: Software mechanisms for power shifting. *IEEE Computer Architecture Letters*, 12(2):67–70, July/December 2013. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [TWI⁺24] **Thomas:2024:BMT**
Samuel Thomas, Kidus Workneh, Ange-Thierry Ishimwe, Zack McKevitt, Phaedra Curlin, R. Iris Bahar, Joseph Izraelewitz, and Tamara Lehman. Baobab Merkle tree for efficient secure memory. *IEEE Computer Architecture Letters*, 23(1):33–36, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [TXD⁺23] **Trochatos:2023:QCT**
Theodoros Trochatos, Chuanqi Xu, Sanjay Deshpande, Yao Lu, Yongshan Ding, and Jakub Szefer. A quantum computer trusted execution environment. *IEEE Computer Architecture Letters*, 22(2):177–180, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [UKM02] **Unsal:2002:CFC**
O. S. Unsal, C. M. Krishna, and C. A. Mositz. Cool-Fetch: Compiler-enabled power-aware fetch throttling. *IEEE Computer Architecture Letters*, 1(1):5, January 2002. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [UTT⁺24] **Ueno:2024:ITB**
Yosuke Ueno, Yuna Tomida, Teruo Tanimoto, Masamitsu Tanaka, Yutaka Tabuchi, Koji Inoue, and Hiroshi Nakamura. Inter-temperature bandwidth reduction in cryogenic QAOA machines. *IEEE Computer Architecture Letters*, 23(1):9–12, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [VD02] **Vandierendonck:2002:ATC**
H. Vandierendonck and K. De Bosschere. An address transformation combining block- and word-interleaving. *IEEE Computer Architecture Letters*, 1(1):8, January 2002. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [VE18] **VandenSteen:2018:MSP**
Sam Van den Steen and Lieven Eeckhout. Modeling superscalar processor memory-level parallelism. *IEEE Computer Architecture Letters*, 17(1):9–12, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [VGMSLN⁺18] **Vakil-Ghahani:2018:CRP** [VMS17]
Armin Vakil-Ghahani, Sara Mahdizadeh-Shahri, Mohammad-**■** Reza Lotfi-Namin, Mohammad Bakhshalipour, Pejman Lotfi-Kamran, and Hamid Sarbazi-Azad. Cache replacement policy based on expected hit count. *IEEE Computer Architecture Letters*, 17(1):64–67, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Vol21]
- [VHN15] **Vandierendonck:2015:EEB**
Hans Vandierendonck, Ahmad Hassan, and Dimitrios S. Nikolopoulos. On the energy-efficiency of byte-addressable non-volatile memory. *IEEE Computer Architecture Letters*, 14(2):144–147, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [VP16]
- [VMP⁺16] **Valero:2016:ELD**
Alejandro Valero, Negar Miralaei, Salvador Petit, Julio Sahuquillo, and Timothy M. Jones. Enhancing the L1 data cache design to mitigate HCI. *IEEE Computer Architecture Letters*, 15(2):93–96, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Verner:2017:EAL**
Uri Verner, Avi Mendelson, and Assaf Schuster. Extending Amdahl’s Law for multi-cores with turbo boost. *IEEE Computer Architecture Letters*, 16(1):30–33, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Volos:2021:CRA**
Haris Volos. The case for replication-aware memory-error protection in disaggregated memory. *IEEE Computer Architecture Letters*, 20(2):130–133, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Verdu:2016:PSA**
Javier Verdu and Alex Pajuelo. Performance scalability analysis of JavaScript applications with Web workers. *IEEE Computer Architecture Letters*, 15(2):105–108, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [VRFT24] **Vieira:2024:GAP**
 João Vieira, Nuno Roma, Gabriel Falcao, and Pedro Tomás. gem5-accel: a pre-RTL simulation toolchain for accelerator architecture validation. *IEEE Computer Architecture Letters*, 23(1):1–4, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [VRS18] **Vijayaraghavan:2018:MBA**
 Thiruvengadam Vijayaraghavan, Amit Rajesh, and Karthikeyan Sankaralingam. MPU–BWM: Accelerating sequence alignment. *IEEE Computer Architecture Letters*, 17(2):179–182, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [VS11] **Vandierendonck:2011:FMM**
 Hans Vandierendonck and Andre Seznec. Fairness metrics for multi-threaded processors. *IEEE Computer Architecture Letters*, 10(1):4–7, January/June 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [WB14] **Wolff:2014:RUR**
 Sonya R. Wolff and Ronald D. Barnes. Revisiting using the results of pre-executed instructions in runahead processors. *IEEE Computer Architecture Letters*, 13(2):97–100, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [WCC14] **Wingbermuehle:2014:OAS**
 Joseph G. Wingbermuehle, Ron K. Cytron, and Roger D. Chamberlain. Optimization of application-specific memories. *IEEE Computer Architecture Letters*, 13(1):45–48, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [WCK08] **Walter:2008:BBE**
 I. Walter, I. Cidon, and A. Kolodny. BENOc: a bus-enhanced network on-chip for a power efficient CMP. *IEEE Computer Architecture Letters*, 7(2):61–64, July 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [WCYC09] **Wang:2009:PST**
 Po-Han Wang, Yen-Ming Chen, Chia-Lin Yang, and Yu-Jung Cheng. A predictive shutdown technique for GPU shader processors. *IEEE Computer Architecture Letters*, 8(1):9–12, January/June 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [WCZ⁺12] **Wang:2012:ISA**
 Yaohua Wang, Shuming Chen, Kai Zhang, Jianghua Wan, Xiaowen Chen, Hu Chen, and Haibo Wang. Instruction

- shuffle: Achieving MIMD-like performance on SIMD architectures. *IEEE Computer Architecture Letters*, 11(2): 37–40, July/December 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [WL16]
- [WJA⁺19] L. Wang, M. Jahre, A. Adileh, Z. Wang, and L. Eeckhout. Modeling emerging memory-divergent GPU applications. *IEEE Computer Architecture Letters*, 18(2):95–98, July 2019. ISSN 1556-6056 (print), 1556-6064 (electronic). [WLDN19]
- [WJFH11] Xiaoqun Wang, Zhenzhou Ji, Chen Fu, and Mingzeng Hu. GCMS: a global contention management scheme in hardware transactional memory. *IEEE Computer Architecture Letters*, 10(1):24–27, January/June 2011. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [WLL17]
- [WKE12] Lisa Wu, Martha A. Kim, and Stephen A. Edwards. Cache impacts of datatype acceleration. *IEEE Computer Architecture Letters*, 11(1):21–24, January/June 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [WLL⁺22]
- [Wu:2016:MCN] Wo-Tak Wu and Ahmed Louri. A methodology for cognitive NoC design. *IEEE Computer Architecture Letters*, 15(1):1–4, January/June 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Weng:2019:DMC] Jian Weng, Sihao Liu, Vidushi Dadu, and Tony Nowatzki. DAEGEN: a modular compiler for exploring decoupled spatial accelerators. *IEEE Computer Architecture Letters*, 18(2):161–165, July 2019. ISSN 1556-6064.
- [Wu:2017:CSB] Hao Wu, Fangfei Liu, and Ruby B. Lee. Cloud server benchmark suite for evaluating new hardware architectures. *IEEE Computer Architecture Letters*, 16(1):14–17, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Wang:2022:CIR] Yinshen Wang, Wenming Li, Tianyu Liu, Liangjiang Zhou, Bingnan Wang, Zhihua Fan, Xiaochun Ye, Dongrui Fan, and Chibiao Ding. Characterization and implementation of radar system applications on a reconfigurable dataflow architecture. *IEEE Computer Architecture Letters*, 21(2):121–124, July/December

2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Wang:2022:ISE**
- [WLN22] Zhengrong Wang, Christopher Liu, and Tony Nowatzki. Infinity Stream: Enabling transparent and automated in-memory computing. *IEEE Computer Architecture Letters*, 21(2):85–88, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Wang:2019:DDD**
- [WLWZ19] Yicheng Wang, Yang Liu, Peiyun Wu, and Zhao Zhang. Detect DRAM disturbance error by using disturbance bin counters. *IEEE Computer Architecture Letters*, 18(1):34–37, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Wu:2023:RAI**
- [WLZZ23] Peiyun Wu, Trung Le, Zhichun Zhu, and Zhao Zhang. Redundant array of independent memory devices. *IEEE Computer Architecture Letters*, 22(2):181–184, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Weston:2023:SLI**
- [WMJM23] Kevin Weston, Farabi Mahmud, Vahid Janfaza, and Abdullah Muzahid. SmartIndex: Learning to index caches to improve performance. *IEEE Computer Architecture Letters*, 22(1):33–36, January/June 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Wang:2017:DAS**
- [WMZY17] Rujia Wang, Sparsh Mittal, Youtao Zhang, and Jun Yang. Decongest: Accelerating super-dense PCM under write disturbance by hot page remapping. *IEEE Computer Architecture Letters*, 16(2):107–110, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Wu:2022:DCG**
- [WSVS22] Lingxi Wu, Rasool Sharifi, Ashish Venkat, and Kevin Skadron. DRAM-CAM: General-purpose bit-serial exact pattern matching. *IEEE Computer Architecture Letters*, 21(2):89–92, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Wu:2021:GOD**
- [WTSW21] Benjamin Wu, Trishita Tiwari, G. Edward Suh, and Aaron B. Wagner. Guessing outputs of dynamically pruned CNNs using memory access patterns. *IEEE Computer Architecture Letters*, 20(2):98–101, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).

- [Wu14] **Wu:2014:ATE**
Carole-Jean Wu. Architectural thermal energy harvesting opportunities for sustainable computing. *IEEE Computer Architecture Letters*, 13(2):65–68, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [WXZ+21] **Wang:2021:WWP**
Lei Wang, Xingwang Xiong, Jianfeng Zhan, Wanling Gao, Xu Wen, Guoxin Kang, and Fei Tang. WPC: Whole-picture workload characterization across intermediate representation, ISA, and microarchitecture. *IEEE Computer Architecture Letters*, 20(2):86–89, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [WYL+15] **Wang:2015:PTM**
Zhaoguo Wang, Han Yi, Ran Liu, Mingkai Dong, and Haibo Chen. Persistent transactional memory. *IEEE Computer Architecture Letters*, 14(1):58–61, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [WYM+16] **Wang:2016:SMF**
Zhenning Wang, Jun Yang, Rami Melhem, Bruce Childers, Youtao Zhang, and Minyi Guo. Simultaneous multi-kernel: Fine-grained sharing of GPUs. *IEEE Computer Architecture Letters*, 15(2):113–116, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [WYY+23] **Wu:2023:CUD**
Meng Wu, Mingyu Yan, Xiaocheng Yang, Wenming Li, Zhimin Zhang, Xiaochun Ye, and Dongrui Fan. Characterizing and understanding defense methods for GNNs on GPUs. *IEEE Computer Architecture Letters*, 22(2):137–140, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [WZLQ15] **Wang:2015:LNV**
Rui Wang, Wangyuan Zhang, Tao Li, and Depei Qian. Leveraging non-volatile storage to achieve versatile cache optimizations. *IEEE Computer Architecture Letters*, 14(1):46–49, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [XCW+19] **Xu:2019:PFD**
Sheng Xu, Xiaoming Chen, Ying Wang, Yinhe Han, Xuehai Qian, and Xiaowei Li. PIMSim: a flexible and detailed processing-in-memory simulator. *IEEE Computer Architecture Letters*, 18(1):6–9, January/June 2019. CODEN ???? ISSN 1556-

6056 (print), 1556-6064 (electronic).

Xie:2022:MSS

- [XGH⁺22] Xinfeng Xie, Peng Gu, Jiayi Huang, Yufei Ding, and Yuan Xie. MPU-Sim: a simulator for in-DRAM near-bank processing architectures. *IEEE Computer Architecture Letters*, 21(1):1–4, January/June 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).

Xie:2019:NXB

- [XHG⁺19] Xinfeng Xie, Xing Hu, Peng Gu, Shuangchen Li, Yu Ji, and Yuan Xie. NNBenchmark: Benchmarking and understanding neural network workloads for accelerator designs. *IEEE Computer Architecture Letters*, 18(1):38–42, January/June 2019. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Xin:2009:ELI

- [XJ09] Jing Xin and Russ Joseph. Exploiting locality to improve circuit-level timing speculation. *IEEE Computer Architecture Letters*, 8(2):40–43, July/December 2009. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Xiao:2007:NPD

- [XL07] X. Xiao and J. Lee. A novel parallel deadlock detection algorithm and hardware

for multiprocessor system-on-a-chip. *IEEE Computer Architecture Letters*, 6(2):41–44, February 2007. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Xu:2014:STM

- [XWG⁺14] Yunlong Xu, Rui Wang, Nilanjan Goswami, Tao Li, and Depei Qian. Software transactional memory for GPU architectures. *IEEE Computer Architecture Letters*, 13(1):49–52, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Xiao:2016:TAC

- [XYMY16] He Xiao, Wen Yueh, Saibal Mukhopadhyay, and Sudhakar Yalamanchili. Thermally adaptive cache access mechanisms for 3D many-core architectures. *IEEE Computer Architecture Letters*, 15(2):129–132, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

Xiao:2015:SCD

- [XYZ15] Canwen Xiao, Yue Yang, and Jianwen Zhu. A sufficient condition for deadlock-free adaptive routing in mesh networks. *IEEE Computer Architecture Letters*, 14(2):111–114, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [Yav24] **Yavits:2024:DCD**
L. Yavits. DRAMA: Commodity DRAM based content addressable memory. *IEEE Computer Architecture Letters*, 23(1):65–68, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Yav24] **Yavits:2024:DCD**
L. Yavits. DRAMA: Commodity DRAM based content addressable memory. *IEEE Computer Architecture Letters*, 23(1):65–68, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YE07] **Yalcin:2007:UTM**
G. Yalcin and O. Ergin. Using tag-match comparators for detecting soft errors. *IEEE Computer Architecture Letters*, 6(2):53–56, February 2007. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YC15] **You:2015:QSA**
Daecheol You and Ki-Seok Chung. Quality of service-aware dynamic voltage and frequency scaling for embedded GPUs. *IEEE Computer Architecture Letters*, 14(1):66–69, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YG18] **Yavits:2018:ASM**
Leonid Yavits and Ran Ginosar. Accelerator for sparse machine learning. *IEEE Computer Architecture Letters*, 17(1):21–24, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YCD⁺20] **Yan:2020:CUG**
Mingyu Yan, Zhaodong Chen, Lei Deng, Xiaochun Ye, Zhimin Zhang, Dongrui Fan, and Yuan Xie. Characterizing and understanding GCNs on GPU. *IEEE Computer Architecture Letters*, 19(1):22–25, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YHM17] **Yasoubi:2017:PEA**
Ali Yasoubi, Reza Hojabr, and Mehdi Modarressi. Power-efficient accelerator design for neural networks using computation reuse. *IEEE Computer Architecture Letters*, 16(1):72–75, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YCH24] **Yang:2024:JIJ**
Yuxin Yang, Xiaoming Chen, and Yinhe Han. JANM-IK: Jacobian argued Nelder-Mead algorithm for inverse kinematics and its hardware acceleration. *IEEE Computer Architecture Letters*, 23(1):45–48, January/June 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YHY⁺22] **Yang:2022:SEP**
Ling Yang, Libo Huang, Run Yan, Nong Xiao, Sheng Ma, Li Shen, and Weixia Xu. Stride equality prediction for value speculation. *IEEE Computer Architecture Letters*, 21(1):45–48, January/June 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).

- [YKZ15] *Letters*, 21(2):57–60, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YJZ15] Fengkai Yuan, Zhenzhou Ji, and Suxia Zhu. Set-granular regional distributed cooperative caching. *IEEE Computer Architecture Letters*, 14(1):75–78, January/June 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YKMG15] Leonid Yavits, Shahar Kvatinsky, Amir Morad, and Ran Ginosar. Resistive associative processor. *IEEE Computer Architecture Letters*, 14(2):148–151, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YKP⁺22] Sungmin Yun, Byeongho Kim, Jaehyun Park, Hwayong Nam, Jung Ho Ahn, and Eojin Lee. GraNDe: Near-data processing architecture with adaptive matrix mapping for graph convolutional networks. *IEEE Computer Architecture Letters*, 21(2):45–48, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Yuan:2015:SGR] Yuan:2015:SGR
- [YMK21] Chao Yu, Sihang Liu, and Samira Khan. MultiPIM: a detailed and configurable multi-stack processing-in-memory simulator. *IEEE Computer Architecture Letters*, 20(1):54–57, January/June 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Yu:2021:MDC] Yu:2021:MDC
- [YMB19] A. Yasin, A. Mendelson, and Y. Ben-Asher. Tuning performance via metrics with expectations. *IEEE Computer Architecture Letters*, 18(2):91–94, July 2019. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Yasin:2019:TPM] Yasin:2019:TPM
- [YMG14] Leonid Yavits, Amir Morad, and Ran Ginosar. Cache hierarchy optimization. *IEEE Computer Architecture Letters*, 13(2):69–72, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Yavits:2014:CHO] Yavits:2014:CHO
- [YNS⁺08] J. H. Yoon, E. H. Nam, Y. J. Seong, H. Kim, B. Kim, S. L. Min, and Y. Cho. Chameleon: a high performance flash/FRAM hybrid solid state disk architecture. *IEEE Computer Architecture Letters*, 7(1):17–20, January 2008. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Yoon:2008:CHP] Yoon:2008:CHP

- [YP23] **Yun:2023:FPP**
Yugyoung Yun and Eunhyeok Park. Fast performance prediction for efficient distributed DNN training. *IEEE Computer Architecture Letters*, 22(2):133–136, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YSL⁺21] **Yoo:2021:MBU**
Mingi Yoo, Jaeyong Song, Jounghoo Lee, Namhyung Kim, Youngsok Kim, and Jinho Lee. Making a better use of caches for GCN accelerators with feature slicing and automatic tile morphing. *IEEE Computer Architecture Letters*, 20(2):102–105, July/December 2021. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YFP14] **Yazdanshenas:2014:CLL**
Sadegh Yazdanshenas, Marzieh Ranjbar Pirbasti, Mahdi Fazeli, and Ahmad Patooghy. Coding last level STT-RAM cache for high endurance and low power. *IEEE Computer Architecture Letters*, 13(2):73–76, July/December 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [yPSS⁺10] **Park:2010:EIP**
Seon yeong Park, Euseong Seo, Ji-Yong Shin, Seungryoul Maeng, and Joonwon Lee. Exploiting internal parallelism of flash-based SSDs. *IEEE Computer Architecture Letters*, 9(1):9–12, January/June 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YQL⁺24] **Yi:2024:GSM**
Shiyan Yi, Yudi Qiu, Lingfei Lu, Guohao Xu, Yong Gong, Xiaoyang Zeng, and Yibo Fan. GATe: Streamlining memory access and communication to accelerate graph attention network with near-memory processing. *IEEE Computer Architecture Letters*, 23(1):87–90, 2024. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YWG17] **Yavits:2017:RAD**
Leonid Yavits, Uri Weiser, and Ran Ginosar. Resistive address decoder. *IEEE Computer Architecture Letters*, 16(2):141–144, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [YYK⁺18] **Yun:2018:RPP**
Ji-Tae Yun, Su-Kyung Yoon, Jeong-Geun Kim, Bernd Burgstaller, and Shin-Dug Kim. Regression prefetcher with preprocessing for DRAM-PCM hybrid main memory. *IEEE Computer Architecture Letters*, 17(2):163–166, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- [YZY⁺22] **Yan:2022:CUH** Mingyu Yan, Mo Zou, Xiaocheng Yang, Wenming Li, Xiaochun Ye, Dongrui Fan, and Yuan Xie. Characterizing and understanding HGNNs on GPUs. *IEEE Computer Architecture Letters*, 21(2):69–72, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic). [ZCG18]
- [ZAK⁺17] **Zhan:2017:CCS** Xin Zhan, Reza Azimi, Svilen Kanev, David Brooks, and Sherief Reda. CARB: a C-state power management arbiter for latency-critical workloads. *IEEE Computer Architecture Letters*, 16(1):6–9, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Zha06]
- [ZB19] **Zhou:2019:QCD** H. Zhou and G. T. Byrd. Quantum circuits for dynamic runtime assertions in quantum computation. *IEEE Computer Architecture Letters*, 18(2):111–114, July 2019. ISSN 1556-6056 (print), 1556-6064 (electronic).
- [ZBA⁺20] **Zhu:2020:HIR** Lingjun Zhu, Lennart Bamberg, Anthony Agnesina, Francky Catthoor, Dragomir Milojevic, Manu Komalan, Julien Ryckaert, Alberto Garcia-Ortiz, and Sung Kyu Lim. Heterogeneous 3D integration for a RISC-V system with STT-MRAM. *IEEE Computer Architecture Letters*, 19(1):51–54, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic). [Zhao:2018:KOA]
- [Zhao:2018:KOA] Wenyi Zhao, Quan Chen, and Minyi Guo. KSM: Online application-level performance slowdown prediction for spatial multitasking GPGPU. *IEEE Computer Architecture Letters*, 17(2):187–191, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Zhang:2006:BIC] **Zhang:2006:BIC** Chuanjun Zhang. Balanced instruction cache: reducing conflict misses of direct-mapped caches through balanced subarray accesses. *IEEE Computer Architecture Letters*, 5(1):2–5, January 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- [Zhou:2006:CFT] **Zhou:2006:CFT** Huiyang Zhou. A case for fault tolerance and performance enhancement using chip multi-processors. *IEEE Computer Architecture Letters*, 5(1):22–25, January 2006. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [Zho06]

- Zhang:2018:RFA**
- [ZKF⁺18] Jiangwei Zhang, Donald Kline, Jr., Long Fang, Rami Melhem, and Alex K. Jones. RETROFIT: Fault-aware wear leveling. *IEEE Computer Architecture Letters*, 17(2):167–170, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zhang:2020:FRP**
- [ZKH⁺20] Jie Zhang, Miryeong Kwon, Sanghyun Han, Nam Sung Kim, Mahmut Kandemir, and Myoungsoo Jung. FastDrain: Removing page victimization overheads in NVMe storage stack. *IEEE Computer Architecture Letters*, 19(2):92–96, July/December 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zidenberg:2012:MHS**
- [ZKW12] Tsahee Zidenberg, Isaac Keslassy, and Uri Weiser. MultiAmdahl: How should I divide my heterogeneous chip? *IEEE Computer Architecture Letters*, 11(2):65–68, July/December 2012. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zha:2017:IFM**
- [ZL17] Yue Zha and Jing Li. IMEC: a fully morphable in-memory computing fabric enabled by resistive crossbar. *IEEE Computer Architecture Letters*, 16(2):123–126, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zha:2018:CRC**
- [ZL18a] Yue Zha and Jing Li. CMA: a reconfigurable complex matching accelerator for wire-speed network intrusion detection. *IEEE Computer Architecture Letters*, 17(1):33–36, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zheng:2018:EPE**
- [ZL18b] Hao Zheng and Ahmed Louri. EZ-Pass: an energy & performance-efficient power-gating router architecture for scalable NoCs. *IEEE Computer Architecture Letters*, 17(1):88–91, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zhao:2017:LIC**
- [ZLAE17] Xia Zhao, Yuxi Liu, Almutaz Adileh, and Lieven Eeckhout. LA-LLC: Inter-core locality-aware last-level cache to exploit many-to-many traffic in GPGPUs. *IEEE Computer Architecture Letters*, 16(1):42–45, January/June 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).

- Zhang:2020:AIG**
- [ZLM⁺20] Zihui Zhang, Jingwen Leng, Lingxiao Ma, Youshan Miao, Chao Li, and Minyi Guo. Architectural implications of graph neural networks. *IEEE Computer Architecture Letters*, 19(1):59–62, January/June 2020. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zhang:2010:FCA**
- [ZLS10] Meng Zhang, Alvin R. Lebeck, and Daniel J. Sorin. Fractal consistency: Architecting the memory system to facilitate verification. *IEEE Computer Architecture Letters*, 9(2):61–64, July/December 2010. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zebchuk:2007:BBC**
- [ZM07] J. Zebchuk and A. Moshovos. A building block for coarse-grain optimizations in the on-chip memory hierarchy. *IEEE Computer Architecture Letters*, 6(2):33–36, February 2007. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zhang:2017:WDP**
- [ZMC17] Dan Zhang, Xiaoyu Ma, and Derek Chiou. Worklist-directed prefetching. *IEEE Computer Architecture Letters*, 16(2):170–173, July/December 2017. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zhang:2023:BPA**
- [ZNTJE23] Shiqing Zhang, Mahmood Naderan-Tahan, Magnus Jahre, and Lieven Eeckhout. Balancing performance against cost and sustainability in multi-chip-module GPUs. *IEEE Computer Architecture Letters*, 22(2):145–148, July/December 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zhang:2018:LHC**
- [ZS18] Guowei Zhang and Daniel Sanchez. Leveraging hardware caches for memoization. *IEEE Computer Architecture Letters*, 17(1):59–63, January/June 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zhu:2014:EWC**
- [ZSLR14] Yuhao Zhu, Aditya Srikanth, Jingwen Leng, and Vijay Janapa Reddi. Exploiting webpage characteristics for energy-efficient mobile Web browsing. *IEEE Computer Architecture Letters*, 13(1):33–36, January/June 2014. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zhou:2022:LPL**
- [ZTRA22] Ranyang Zhou, Sepehr Tabrizchi, Arman Roohi, and Shaahin

- Angizi. LT-PIM: an LUT-Based Processing-in-DRAM architecture with RowHammer self-tracking. *IEEE Computer Architecture Letters*, 21(2):141–144, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic). [ZWT22]
- Zhang:2016:SIW**
- [ZTS16] Chulian Zhang, Hamed Tabkhi, and Gunar Schirner. Studying inter-warp divergence aware execution on GPUs. *IEEE Computer Architecture Letters*, 15(2):117–120, July/December 2016. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zhang:2003:WHC**
- [ZVYW03] Chuanjun Zhang, F. Vahid, Jun Yang, and W. Walid. A way-halting cache for low-energy high-performance systems. *IEEE Computer Architecture Letters*, 2(1):5, January 2003. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zheng:2015:ACC**
- [ZWL15] Zhong Zheng, Zhiying Wang, and Mikko Lipasti. Adaptive cache and concurrency allocation on GPGPUs. *IEEE Computer Architecture Letters*, 14(2):90–93, July/December 2015. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic). [ZZW⁺23]
- Zhu:2022:RBP**
- Yongye Zhu, Shijia Wei, and Mohit Tiwari. Revisiting browser performance benchmarking from an architectural perspective. *IEEE Computer Architecture Letters*, 21(2):113–116, July/December 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zokae:2018:APM**
- Farzaneh Zokae, Hamid R. Zarandi, and Lei Jiang. Aligner: a process-in-memory architecture for short read alignment in ReRAMs. *IEEE Computer Architecture Letters*, 17(2):235–238, July/December 2018. CODEN ???? ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zou:2022:AGP**
- [ZZW⁺22] Mo Zou, Mingzhe Zhang, Rujia Wang, Xian-He Sun, Xiaochun Ye, Dongrui Fan, and Zhimin Tang. Accelerating graph processing with lightweight learning-based data reordering. *IEEE Computer Architecture Letters*, 21(1):5–8, January/June 2022. ISSN 1556-6056 (print), 1556-6064 (electronic).
- Zhao:2023:RAL**
- Xia Zhao, Guangda Zhang, Lu Wang, Yangmei Li, and Yongjun Zhang. RouteReplies: Alleviating long latency in many-chip-module GPUs.

IEEE Computer Architecture Letters, 22(1):29–32, January/June 2023. ISSN 1556-6056 (print), 1556-6064 (electronic).